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0.13-μm CMOS Vector Modulator for Wireless Backhaul System

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***Abstract*—**In this paper, a CMOS vector modulator designed for wireless backhaul system based on 802.11ac is presented. A poly phase filter and sign select switches yield two orthogonal signal paths. Two variable gain amplifiers with strongly reduced phase shift of only ±5 ° are used to weight these paths. It has a phase control range of 360 ° and a gain range of -10 dB to 10 dB. The current drawn from a 1.2 V supply amounts 20.4 mA. Using a 0.13 μm technology, the chip die area amounts 1.47x0.75 mm².

***Keywords*—**CMOS, vector modulator, backhaul, 802.11ac.

I. Introduction

MIMO systems have been widely known as a promising technology that offers significant spectral efficiency gains. When the capacity of modern communications is concerned, the sum rate scaling of down-link in the broadcast channel can be attained by having M antenna elements at the base station, even with a single antenna at the mobile terminals [1], [2]. The demands for high data rates and vast coverage ranges of current and evolving wireless applications are growing continuously. To satisfy these needs, new concepts beyond existing wireless technologies have to be developed while still being compliant with the bandwidth regulations and compatible to former systems. One promising approach is to exploit the benefits of spatial diversity and beamforming. Employing these techniques, a higher signal-to-noise-ratio is achievable thus enabling the system to use more sophisticated data modulation schemes and therefore to increase the data rate.

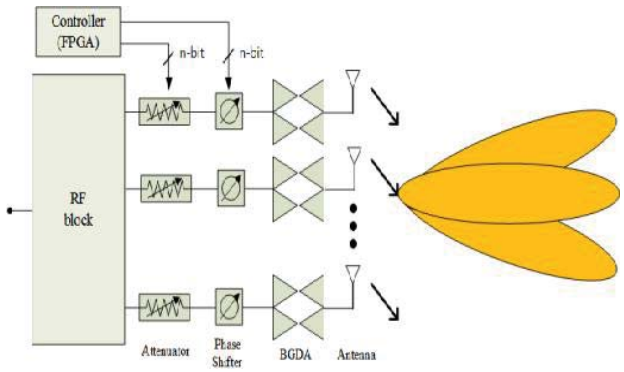

Fig 1 RF beam forming system

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Recent works [3], [4] demonstrated the feasibility to perform the complex weighting required for spatial diversity in the radio frequency (RF) domain. As depicted in Fig. 1, the weighting can be realized by means of a phase shifting circuit along with a variable gain amplifier or attenuator, respectively.

Vector modulators are a good alternative, because they allow for direct manipulation of the real and imaginary part of the signal. Besides, they can be easily calibrated. Several works like [5]-[8] presented vector modulating radio frequency integrated circuits based on GaAs technologies. Although providing good results, these circuits cannot compete with CMOS realizations in terms of costs for mass fabrication. Another publication [9] showed a CMOS vector modulator only being able to steer the phase of the vector.

This work is intended to control both gain and phase in one circuit using a standard 0.13 μm CMOS technology. The system architecture is shown in Section II. Section III focuses on the particular parts of the system and results are presented in Section IV.

II. System Architecture

To keep compliance with standard 802.11ac, the vector modulator was designed in a way that it can be inserted as a module in a conventional topology. The proposed vector modulator is shown in Fig. 2. Resulting from requirements of the whole wireless backhaul system, the output of the vector modulator is double ended.

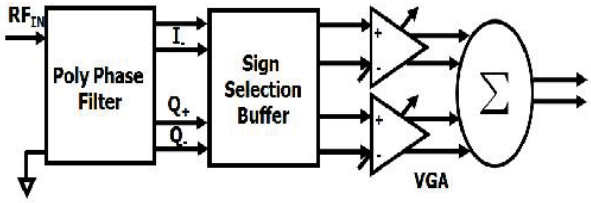

Fig. 2 System architecture of the proposed vector modulator

The signal is located in the complex plane by adding two orthogonal, properly weighted vectors together. The vectors are generated by the vector modulator. A poly phase filter is used as an input divider and phase offset generator.

The poly phase filter provides differential in phase and quadrature components at its output, yielding four paths with a phase shift of 0°, 180°, 90° and 270°, respectively. By means of CMOS switches, the quadrant of the final vector is chosen while terminating the other two unused paths. A termination impedance similar to the input impedance of the VGA ensures constant load of the poly phase filter. Both selected orthogonal

vectors are then weighted in magnitude by VGAs and, finally, added together by a combiner. By employing two amplifiers, the control complexity can be reduced significantly compared to prior designs using three or even four controllable paths.

III. Circuit Design

A. Poly Phase Filter

Recent works designed in GaAs technology, use independent high pass and low pass branches for generating the phase offsets of the vector modulator paths. Unfortunately, these branches would not provide enough phase accuracy in CMOS technologies, because of larger absolute process tolerances and worse substrate isolation.

In this work, a poly phase filter is used to generate the necessary in phase and quadrature components. In order to get wanted center frequency, LC product should be exact number. Since L & C magnitude variations are more than 20% easily on silicon, LC time constant needs to be calibrated and modified by changing C-bank control bits. Basic idea of calibration is to compare LC delay time with reference Lref Cref delay time. Charge Pump charges or discharges on Cload for the time constant difference between L, C and Lref, Cref. Lref and Cref are external +/-1% components. Initially, the Vout DC is set to Vref. At positive or negative clock edge, Vout is charged or discharged from Vref and final Vout after 5~10 clock time period (can be programmed) is stored. Search it for the best C-bank state close to initial Vref. The circuit schematic is shown in Fig. 3 and the simulation result is shown in Fig. 4.

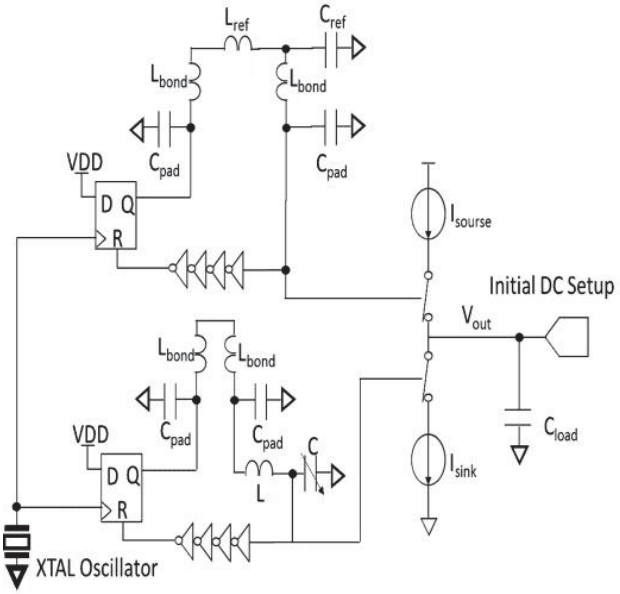

Fig. 3 Poly phase filter with calibration circuits

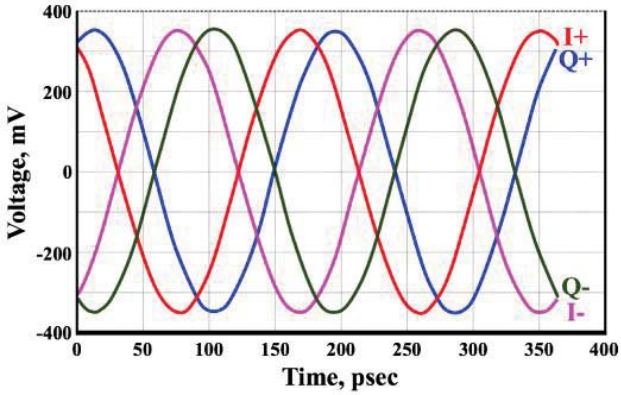

Fig. 4 Simulation result of poly phase filter

B. Switches

The quadrant selection switches should, if switched on, yield an approximate loss of 3 dB to still reach enough gain at the output. Also, in off-state, attenuation should be better than 20 dB to suppress the unwanted paths sufficiently. Each signal path can be either switched to its corresponding VGA input or to a dummy load by means of CMOS transfer gates. To achieve high linearity without any additional power consumption, the drain to source voltage of all transistors is set to zero via high-ohmic resistors [9], making it unlikely to drive the transistor into its active region and adding nonlinearities to the signal.

C. Variable Gain Amplifier

For weighting the paths, two variable gain amplifiers are needed. To achieve high accuracy of the output vector, it is necessary to reduce phase variations to a minimum with respect to the varied gain.

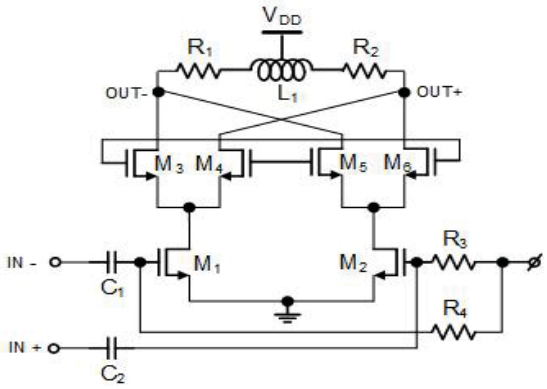

Fig. 5 Variable gain amplifier topology

Its simplified topology is shown in Fig. 5. The schematic is based on a cascode stage and consists of M_1, M_2 as a common source stage and two common gate stages M_3, M_6 in parallel. The differential outputs are at the drain of M_4, M_5. It is shown by simulations in that this amplifier has a phase variation of only ±3.5 ° while covering a gain control range of 20 dB. These properties make it the ideal choice for the use in a vector

modulator. The simulation result is shown in Fig. 6. The VGA gain is between -10 dB and 10dB.

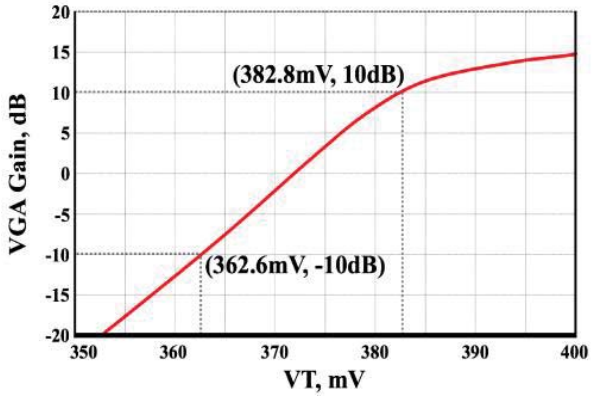

Fig. 6 Simulation result of VGA gain

The complete monolithic circuit was designed using a 0.13 µm technology. The core size without pads is 1.47x0.75 mm². A chip layout is shown in Fig. 7.

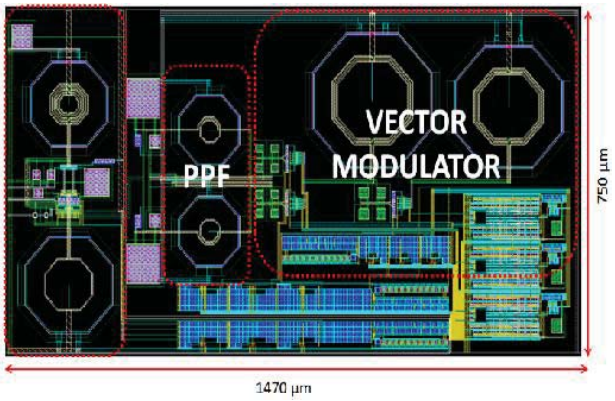

Fig. 7 Layout of vector modulator

IV. Results

The results of the vector modulator presented in this paper were simulated by circuit simulator. The circuit draws a maximum current of 20.4 mA from a 1.2 V supply. The RMS (Route Mean Square) attenuation error of the vector modulator when varying the control voltages is shown in Fig. 8. Fig. 9 shows the simulated RMS phase error. Minimal phase variations occur at control voltages of 0.1 V and above. At this point, the corresponding gain is about -20 dB. The simulated RMS attenuation error stays in the same error bound of 0.3 dB. Also, the simulated RMS phase error stays in the same error bound of 3 °. Figs. 10-13 show the delta phase at around 5GHz - 6GHz. The minimum phase is 2.6° and the maximum phase difference is 1.7° at 44.95°.

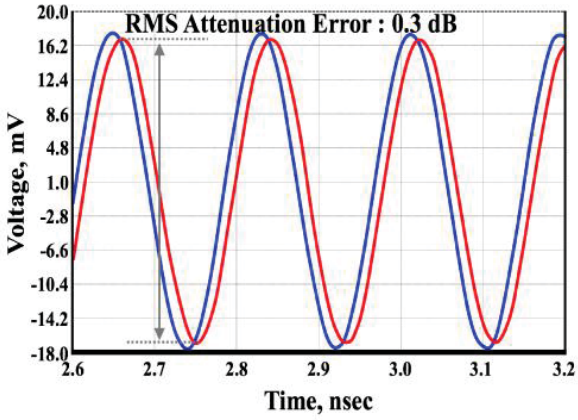

Fig. 8 Simulation result of RMS attenuation error

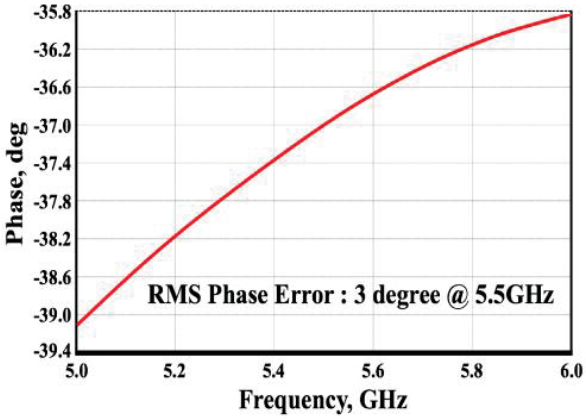

Fig. 9 Simulation result of RMS phase error

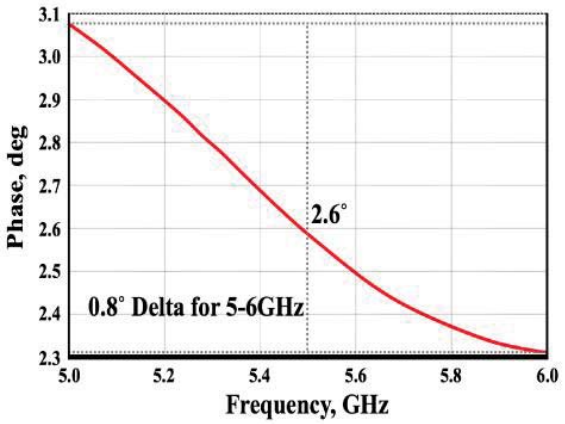

Fig. 10 Simulation result of phase difference at 2.6°

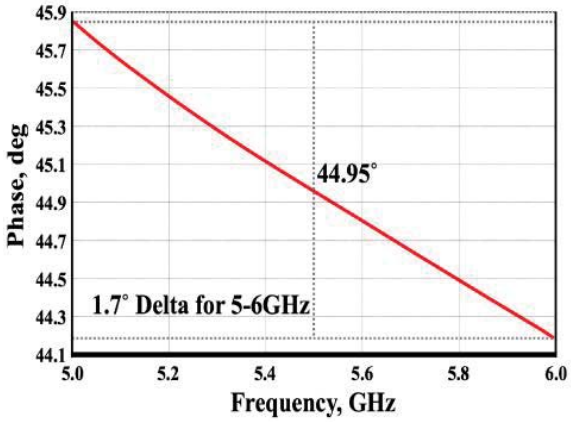

Fig. 11 Simulation result of phase difference at 44.95°

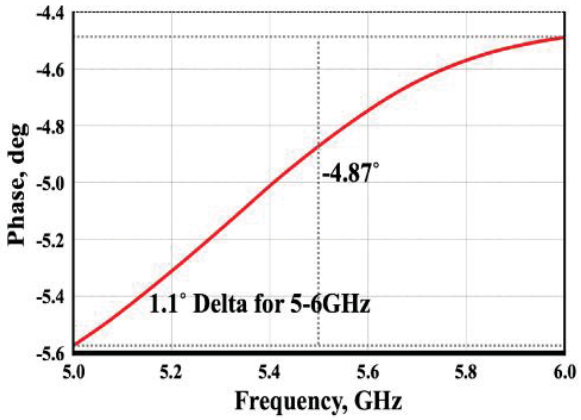

Fig. 12 Simulation result of phase difference at -4.87°

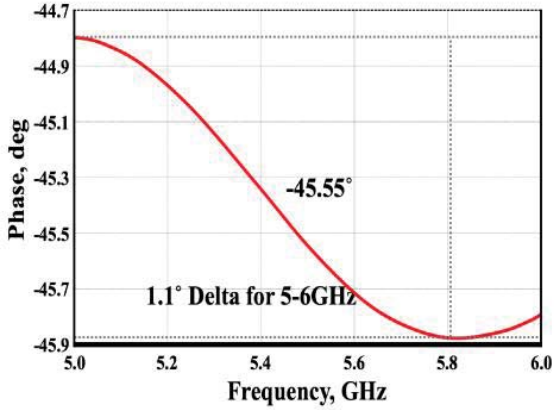

Fig. 13 Simulation result of phase difference at -45.55°

V. Conclusion

This work presented the design of a fully integrated vector modulator using a standard 0.13 µm CMOS technology. The particular components needed for the chosen topology were selected according to the system requirements. It was shown that gain and phase of the signal can be controlled individually. The RF imperfections were reduced to a minimum by employing variable gain amplifiers with low phase variations thus reducing the efforts for linearization and calibration circuitry. This vector modulator is compatible to 802.11ac wireless backhaul systems.

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References

[1] G. Caire, S. Shamai, "On the achievable throughput of a multiantenna Gaussian broadcast channel," *IEEE Trans. Inf. Theory*, vol. 49, pp.1691-1706, 2003.
[2] H. Huang, C. B. Papadias, S. Venkatesan, MIMO Communication for cellular Networks. Springer, 2012.
[3] A. Hajimiri, H. Hashemi, A. Natarajan, X. Guan, and A. Komijani, "Integrated phased array systems in silicon", Proceedings of IEEE, vol. 93, no. 9, pp. 1637–1655, 2005.
[4] J. Paramesh, R. Bishop, K. Soumyanath, and D. Allstot, "A four-antenna receiver in 90-nm CMOS for beamforming and spatial diversity", IEEE Journal of Solid-State Circuits, vol. 40, no. 12, pp. 2515–2524, 2005.
[5] F. Ellinger, R. Vogt, and W. Bächtold, "A high yield ultra small passive vector modulator based phase shifter for smart antenna combining at C-band", *IEEE/CSIRO Asia Pacific Microwave Conference*, pp. 794–797, Dec. 2000.
[6] F. Ellinger, U. Lott, and W. Bächtold, "An antenna diversity MMIC vector modulator for HIPERLAN with low power consumption and calibration capability", *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, pp. 964– 969, May 2001.
[7] F. V. D. Bogaart and R. Pyndiah, "A 10-14 GHz linear MMIC vector modulator with less than 0.1 dB and 0.8 ° amplitude and phase error", *IEEE MTT-S Digest*, pp. 465–468, 1990.
[8] J. Grajal, J. Gismero, M. Mahfoudi, and F. A. Petz, "A 1.4- 2.7 GHz analog MMIC vector modulator for a crossbar beamforming network", *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, pp. 1705–1714, Oct. 1997.
[9] K.-J. Koh and G. M. Rebeiz, "0.13 µm CMOS phase shifters for X-, Ku-, and K-band phased arrays", *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 2535-2545, Nov. 2007.

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