International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:10, No:3, 2016

A 5-V to 30-V Current-Mode Boost Converter with Integrated Current Sensor and Power-on Protection

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***Abstract*—**This paper presents a 5-V to 30-V current-mode boost converter for powering the drive circuit of a micro-electro-mechanical sensor. The design of a transconductance amplifier and an integrated current sensing circuit are presented. In addition, essential building blocks for power-on protection such as a soft-start and clamp block and supply and clock ready block are discussed in details. The chip is fabricated in a 0.18-μm CMOS process. Measurement results show that the soft-start and clamp block can effectively limit the inrush current during startup and protect the boost converter from startup failure.

***Keywords*—**Boost Converter, Current Sensing, Power-on protection, Step-up Converter, Soft-start.

I. Introduction

NOWADAYS, most of the integrated circuit (IC) chips are digital-intensive [1], [2]. Power consumption of these IC chips reduces by using lower supply voltages. On the other hand, high supply voltages are often required by interfaces to external devices such as micro-electro-mechanical system (MEMs) devices. Hence, power management units containing low dropout regulator (LDO), bandgap voltage reference, boost converters are becoming almost essential for every System-on-Chip design. This paper presents a 5-V to 30-V boost converter, which is designed to work in continuous conduction mode (CCM) and aimed to power the high-voltage driver circuit with a specified load current range from 5 mA to 20 mA. The boost converter is part of a MEMs sensor interfacing chip. The block diagram of the current-mode boost converter is illustrated in Fig. 1. The 1-MHz clock signal is generated by the digital control module of the sensor interfacing circuit which is powered by a 1.8-V on-chip LDO.

The behavior of boost converters has been well analyzed and the design procedures are also well reported in many application notes [3]-[5]. In [5], it has been pointed out that power-on protection circuits are very important for boost converter, as any current or voltage overshoot could damage the chip. However, there are few papers discussing the design of these essential protection circuits.

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This work is supported by Physical Logic Ltd. Israel.

The paper is organized in the following matter. Section II shows overall circuit structure of the boost converter, Section III on the design of the soft-start and clamp block and the Supply and Clock Ready (SCR) block for power-on protection, Section IV on the measurement and Section V is the conclusion.

II. System Architecture

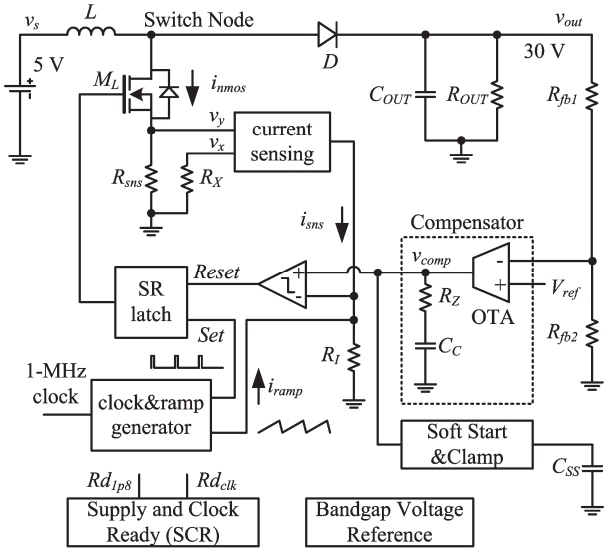

Fig. 1 Block diagram of the current-mode boost converter

As shown in Fig. 1, the widely used peak-current control topology is adopted in this design. The current sensing block combined with the sensing resistor R_{sns} and scaling resistor R_X are employed to generate the feedback current signal i_{sns}, which is proportional to the current flowing through the N-type power transistor M_L. The output voltage is fed back through a voltage divider to the negative input of the transconductance amplifier (OTA). The OTA with the resistor R_Z and capacitor C_C forms a gm-C filter to compensate the loop gain of the boost converter. The clock and ramp generator is used to generate the *set* signal for the SR latch as well as the compensation ramp required for preventing sub-harmonic oscillation. The soft-start and clamp block is used to prevent excessive output voltage overshoot at startup as well as limiting the maximum current flowing through M_L. The supply and clock ready (SCR) block is designed for checking the availability of the on-chip generated 1.8-V supply and 1-MHz clock to prevent any fault switching of the power transistor during the power-on period.

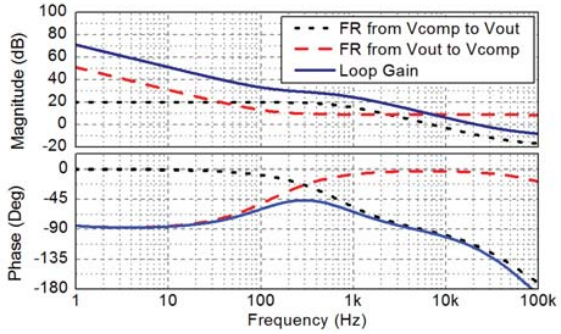

Fig. 2 Bode Diagram of the loop gain of the boost converter

The linearized loop gain of the boost converter is plotted in Fig. 2. For current-mode control, the frequency response (FR) from OTA output v_{comp} to boost converter output v_{out} has one dominant pole at low frequency and an inherent right-half-plane zero at high frequency (the black dot curve in Fig. 2). Since the frequency of the zero depends on load resistance R_{OUT} and inductor value as well as the supply and output voltages, the minimum supply voltage and R_{OUT} should be used when designing the compensator (e.g., 4.5 V and 1.5 kΩ in this design). The frequency response of the compensator with the feedback voltage divider is plotted as the red dash curve on Fig. 2. The compensator shifts up the loop gain and hence expends its bandwidth (the blue solid curve in Fig. 2). The unity gain bandwidth of the boost converter is 22 kHz.

III. Design of Circuit Blocks

A. Operational Transconductance Amplifier (OTA)

The circuit schematic of the OTA is shown in Fig. 3, which is the critical building block of the boost converter. The design consideration includes the transconductance g_m, output resistance and output swing. Low power consumption is also essential to achieve a high overall efficiency. Consequently, the folded-cascode structure is adopted here. The simulated g_m is 264 μA/V and the output resistance of the OTA is larger than 378 MΩ. It may be worthwhile to highlight that the transistors M_{11}-M_{17} are 1.8-V devices. By replacing the thick-oxide 5-V transistors with the thin-oxide 1.8-V transistors, the output swing of the OTA is maximized.

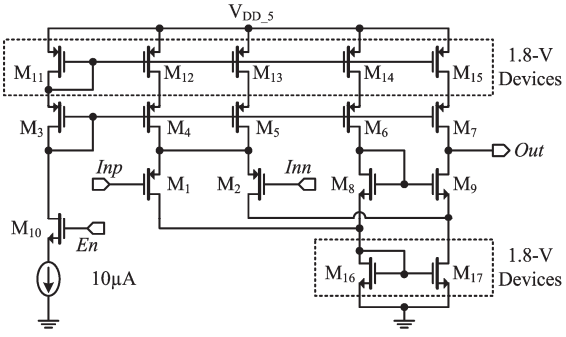

Fig. 3 Circuit schematic of the folded-cascode OTA

B. Current Sensing Block

The current sensing block is designed based on the matched current source technique presented in [6]. A 200-mΩ sensing resistor R_{sns} is put in series with the power transistor M_L with a 200-Ω scaling resistor R_X placed side by side. The current sensing circuit intents to force the voltage at nodes v_x and v_y to be same and hence the output current i_{sns} is proportional to i_{nmos}. The small signal current sensing gain A_I is calculated as

$$A_I = \frac{i_{sns}}{i_{nmos}} = \frac{R_{sns}}{R_X} \cdot \frac{1}{1 + \frac{(1+g_{m24}R_X)(1+g_{m18}R_{sns})}{g_{m18}g_{m24}r_{o20}R_X}} \quad (1)$$

C. Supply and Clock Ready Block

The whole MEMs sensor interfacing chip is powered by a regulated 5-V supply. The on-chip LDO generates the 1.8-V supply for the digital module of the chip. The digital module generates the 1-MHz clock required by the boost converter. To prevent any fault turning-on of the power transistor during the power-on period, the boost converter should operate only after the on-chip generated 1.8-V supply is stabilized and the clock signal is available. Hence, a Supply and Clock Ready (SCR) block has been proposed to generate two flag signals for the main boost converter control circuit, which are the clock-ready signal Rd_{clk} and 1.8-V supply ready signal Rd_{1p8}.

The circuit schematic of the proposed SCR block is shown in Fig. 4. When the LDO output approaches to 1.8 V, the drain voltage of the nMOS is pulled down and the output Rd_{1p8} goes to 5 V, which indicates the 1.8-V supply is ready. At the same time, a pulse signal is generated by the pulse generator to reset the Rd_{clk} output signal to 0 V. Recall that the clock signal is assumed to arrive only after the 1.8-V supply is stabilized. The 1-MHz clock signal will toggle the SR-latch and set the Rd_{clk} output signal to 5V, which indicates the clock signal is ready. This block can be bypassed by shorting the *enable* input, *En*, to ground, otherwise the *enable* signal is charged to 5 V by an internal pull-up resistor. Fig. 5 illustrates the typical signal waveforms of the SCR block. The signal Rd_{1p8} toggles to logic high when the 1.8-V supply is higher than 1.5 V. The Rd_{clk} signal rises to logic high when the clock signal is available. Monte-Carlo simulation has to be conducted to ensure this block works functionally at different process variation and parameter mismatch.

D. Soft-start and Clamp Block

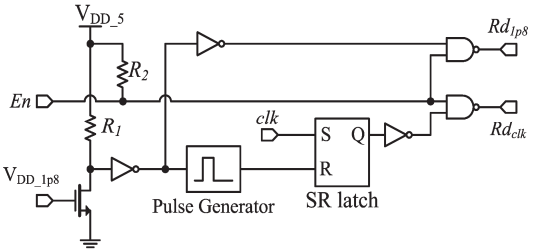

Fig. 4 Circuit schematic of the SCR block

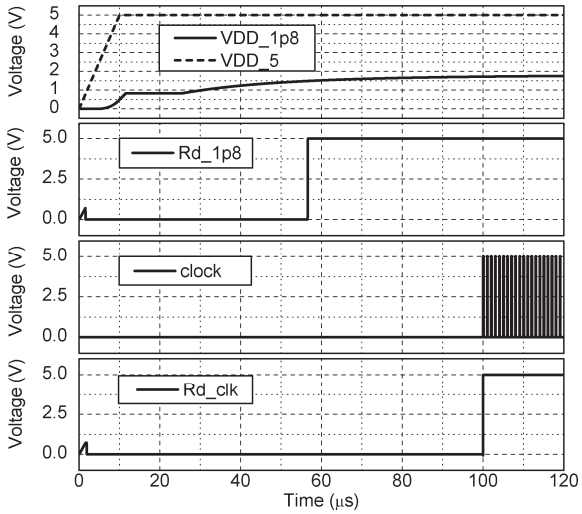

Fig. 5 Simulated signal waveforms of the SCR block

It is important for boost converters to have a soft-start behavior that limit the inrush current and prevent excessive output voltage overshoot at startup. In this work, the proposed soft-start and clamp block is added at the output of the OTA. The circuit schematic is shown in Fig. 6. For the flag signal Rd_{clk} at logic low, the gate voltage of the pMOS transistor M_C, is pulled down to 0 V by the current mirror and the output voltage of the OTA is bounded at a threshold voltage above ground. When Rd_{clk} rises to logic high, indicating the boost converter can start operating, the current flows through R_{SS} to charge up the soft-start capacitor C_{SS}. The soft-start voltage V_{SS} rises, so does the output of the OTA v_{comp}. The soft-start performance of the boost converter can be adjusted by the changing the size of the external C_{SS}. This block is also used to clamp the maximum output voltage of the OTA, indirectly limits the maximum current flowing through the power transistor. The maximum value of V_{SS} is adjusted by tuning the number and size of the diode-connected pMOS transistors. This soft-start and clamp block can be put out of action by setting the pin *Disable* to logic high, which pulls the gate voltage of M_C to 5 V.

Fig. 7 illustrates the effect of the soft-start and clamp block on restraining the output swing of the OTA when the Rd_{clk} signal is at logic high. The negative input of the OTA is swept from -1 mV to 0.5 mV with respect to the 1.2-V positive input. As shown on Fig. 7, when the soft-start and clamp block is active, the maximum output voltage of the OTA is restrained to 4 V. The maximum current flowing through M_L can be calculated based on (2). In this design, the current to voltage conversion resistor R_I is 10 kΩ. The current sensing gain A_I is roughly 0.001 and the peak ramp current I_{ramp_max} is 150 μA. As a result, the maximum current flowing through M_L is limited to 0.25 A.

$$I_{nmos\_max} = \left(v_{comp\_max} / R_I - i_{ramp\_max}\right) / A_I \qquad (2)$$

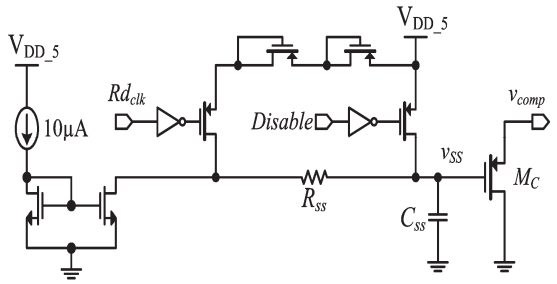

Fig. 6 Circuit schematic of the soft-start and clamp block

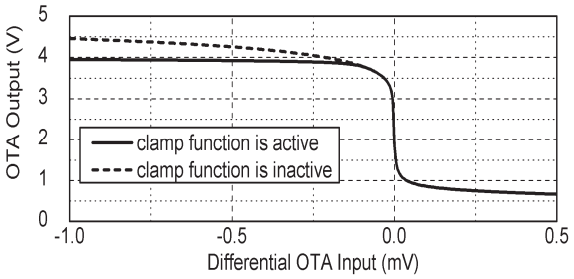

Fig. 7 Output swing of OTA with/without soft-start and clamp block

IV. Measurement

The 5-V to 30-V boost converter is tested based on the fabricated test chip, which contains the boost converter and a high-voltage driver. The micro-photograph of the test chip is shown Fig. 8. The layout of the boost converter is optimized for the integration chip, rather than this test chip, Hence, a large amount of space on this test chip are unused and filled by metals. The core of the boost converter, which is cycled by the dash line on Fig. 8, occupies an area of 0.48 mm^2. A printed circuit board has been designed for testing the boost converter. The surface-mount inductor is 100 μH and the output capacitor is a 330-nF ceramic capacitor in 1206 case.

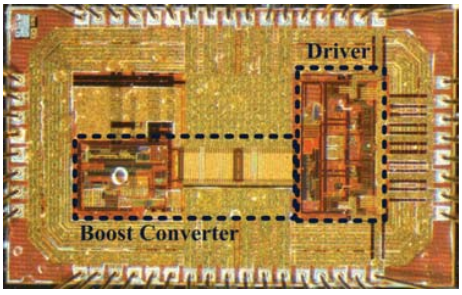

Fig. 8 Micro-photograph of the boost converter

Fig. 9 plots the signal waveforms of the boost converter during power-on period. The boost converter was first powered up by the 5-V supply, and then the clock signal was activated. The soft-start capacitor used in this test is 8.2 nF and the load resistor is 6 kΩ. The acquirement of the waveforms is triggered by the rising edge of the 1-MHz clock signal, which was plotted on Channel 4 of the oscilloscope. Channel 1 plots the output voltage of the boost converter. Before the clock signal is activated, the output of the boost converter states at about 4.3V,

a diode voltage drop from 5-V supply. When the clock signal is activated, the output voltage ramps to 30 V in a controlled manner without any overshoot. Channel 3 plots the current flowing through the inductor. The maximum transient current is 134 mA, which is 88-mA higher than the average inductor current at steady-state condition, but well below the designed current limit (i.e., 0.25 A). Channel 2 plots the voltage across the soft-start capacitor C_{SS}.

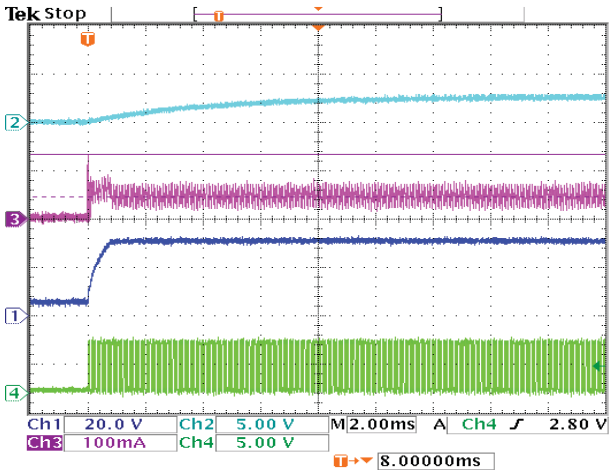

Fig. 9 Start-up waveforms, Css = 8.2 nF

Fig. 10 shows the captured signal waveforms of the boost converter in steady-state condition. The load current is set to 5 mA, which is the minimum specified load current. Channel 1 plots the output voltage of the boost converter. Channel 2 plots the voltage at the switching node. Channel 3 plots the inductor current, which keeps above 0 A, and hence proves that the boost converter always works in continuous conduction mode. Channel 4 plots the external 1-MHz clock signal as the triggering signal.

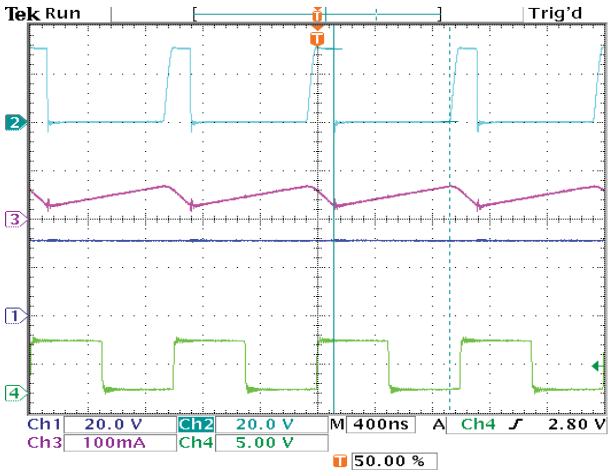

Fig. 10 Switching waveform at 5-mA load condition

The experimental performance of the boost converter is summarized in Table I. Due to the flicker noise of the integrated 1.2-V bandgap voltage reference, the boost converter output varies slightly with time. For instance, an 80-μV variation on the output of the 1.2-V reference, which is a practical value for low-power voltage reference design, can cause a 2-mV variation in the boost converter output voltage. As a result, line regulation and load regulation results are measured at low frequency, rather than at DC. Similarly, the output voltage variation over temperature is also limited by the performance of the bandgap voltage reference.

TABLE I
SUMMARY OF MEASUREMENT RESULTS

Parameter	Conditions	Meas. Result
$\Delta V_{out}/\Delta T$	Temp. varies from -40 °C to 85 °C, I_{load} = 5 mA	-1.75 mV/°C
Efficiency	At max. load 20 mA	80 %
V_{out} ripple	At max. load 20 mA	107 mV
Line regulation	V_{out} = 30V, R_{load} = 6 kΩ, Supply voltage switches between 4.5V and 5.5V at 1 kHz.	33.7 mV/V
Load regulation	V_S = 5V, Load current switches between 5 mA and 20 mA at 120 Hz.	-0.116V/A

V. Conclusion

This paper presents a current-mode boost converter integrated on a MEMs sensor interfacing chip. The design of the OTA and current sensing blocks are detailed. In addition, based on the signal arriving sequence of the integration chip, the soft-start and clamp circuit and supply and clock ready block have been developed for power-on protection. The fabricated chip has been tested successfully. Measurement results show that the soft-start and clamp block can effectively limit the inrush current during startup and protect the boost converter from startup failure.

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