

A Digital Pulse-Width Modulation Controller for High-Temperature DC-DC Power Conversion Application

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Abstract—This paper presents a digital non-linear pulse-width modulation (PWM) controller in a high-voltage (HV) buck-boost DC-DC converter for the piezoelectric transducer of the down-hole acoustic telemetry system. The proposed design controls the generation of output signal with voltage higher than the supply voltage and is targeted to work under high temperature. To minimize the power consumption and silicon area, a simple and efficient design scheme is employed to develop the PWM controller. The proposed PWM controller consists of serial to parallel (S2P) converter, data assign block, a mode and duty cycle controller (MDC), linearly PWM (LPWM) and noise shaper, pulse generator and clock generator. To improve the reliability of circuit operation at higher temperature, this design is fabricated with the 1.0- μm silicon-on-insulator (SOI) CMOS process. The implementation results validated that the proposed design has the advantages of smaller size, lower power consumption and robust thermal stability.

Keywords—DC-DC power conversion, digital control, high temperatures, pulse-width modulation.

I. INTRODUCTION

NOWADAYS, battery powered systems are widely used in a variety of portable applications, such as mobile phone and notebook. For some mobile devices, in order to deliver large power to their loads, such like speakers, motors and various transducers, it is quite usual that the system requires supply voltages that are much higher than the input voltage. For instance, to drive Radio Frequency (RF) and analog circuits in a battery powered system, the required output voltage swing may be as high as 24 V, but the battery used can normally supply only 5 V or lower input voltage.

The straight forward solution for such applications is to use a buck-boost DC-DC converter which is able to generate an output voltage higher than the supply voltage, whose conceptual diagram is shown in Fig. 1. Therefore, in recent years, different research on buck-boost DC-DC converters [1], [2], has been reported. However, as so far, buck-boost DC-DC converters for high-temperature applications are few. Whereas in today's oil and gas industry, high-temperature electronics are desired. For example, in order to explore deeper reservoirs, high-temperature electronic devices are demanded during the Measurement While Drilling (MWD) application of the oil drilling services [3]. Thus, this research is specially focused on a digital control based design which can work under high temperature to generate an output signal with voltage higher

than the supply voltage.

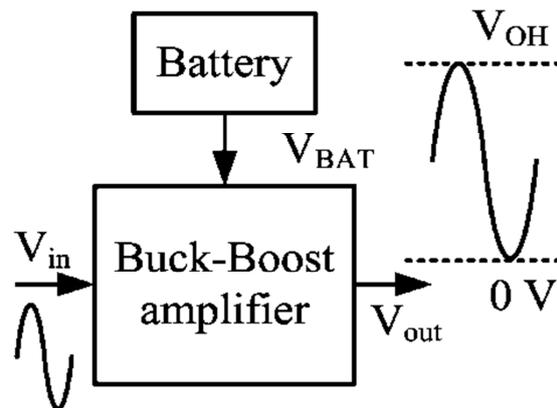


Fig. 1 Conceptual diagram of buck-boost DC-DC converter

In a buck-boost DC-DC converter, a non-linear pulse-width modulator is required, since the transfer function from duty cycle to output is no longer linear. For example, in [1], the non-linear pulse-width modulator is built using analog circuit by employing an exponential carrier generator. Compared with analog controller, many advantages such as lower power and silicon areas consumption and more flexible control capability can be achieved using digital controller [4]. Therefore, when the digital control signal is available, a fully digital controller is suitable for DC-DC power conversion application [5].

In this work, a SOI-based digital non-linear PWM controller in a HV buck-boost DC-DC converter for the piezoelectric transducer of the down-hole acoustic telemetry system is present. With the SOI process, the reliability of circuit operation at higher temperature can be improved [6]. Additionally, when combined with digital controller, the system can achieve high power efficiency and hence long battery life which is essential in portable applications.

In this section, a brief overview of this research is given. The rest of this paper is structured as follows. In Section II, the system architecture of the proposed buck-boost DC-DC converter is introduced. Section III describes the functions of the non-linear PWM controller and the control scheme for buck-boost DC-DC converter. Hardware implementation and validation results of the proposed design are presented in Section IV. Finally, the conclusions are drawn in Section V.

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II. PROPOSED BUCK-BOOST CONVERTER WITH DIGITAL CONTROLLER

The architecture of the proposed buck-boost converter with digital controller is shown in Fig. 2. The system consists of the Buck Cascaded Buck-Boost (BuCBB) power stage with the input voltage from battery, the digital pulse-width modulator (DPWM) that convert the sensor collected data to be transmitted to the surface to a modulated pulse waveform output and the HV transducer driver which use the output pulse signal as input to generate an amplified PWM signal. The buck-boost DC-DC converter uses the proposed PWM controller with independent controlled power transistors to reduce the component stress as well as to reduce the size of the integrated chip. With independent controlled buck and boost power stages, the output voltage can be either higher or lower than the supply voltage.

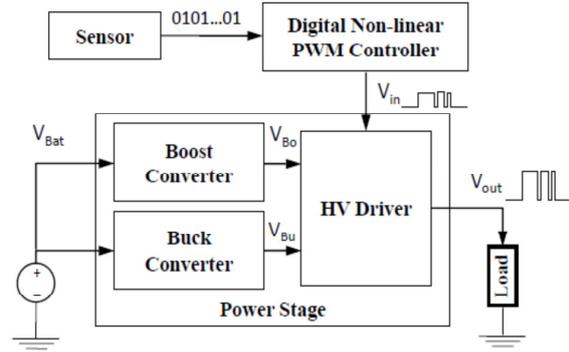


Fig. 2 System architecture of an acoustic transmitter for well-drilling application

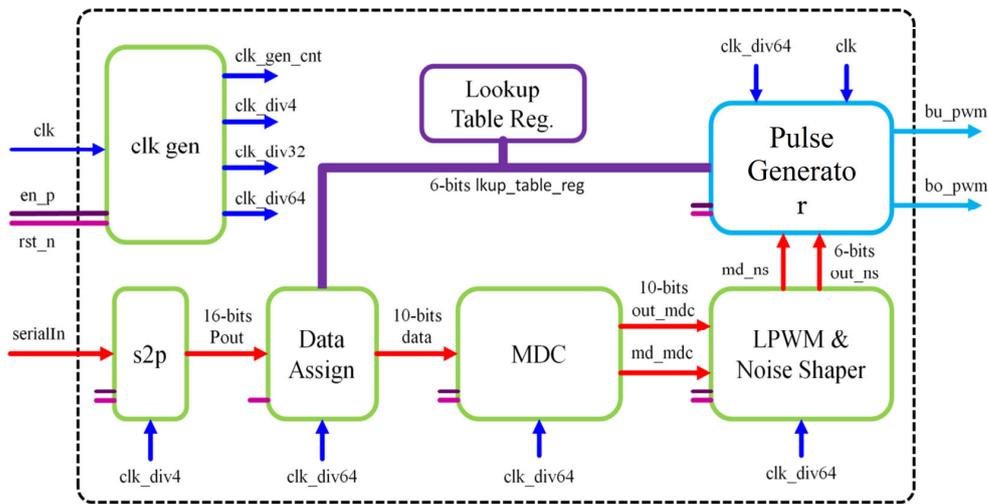


Fig. 3 Block Diagram of digital non-linear PWM controller

The proposed buck-boost converter has two operating modes: buck mode and the boost mode. The `pwm_bu` and `pwm_bo` for the buck power stage and the boost power stage are independently generated pulse signals by the proposed non-linear pulse-width modulator. These operation modes are significant for the down-hole acoustic telemetry system. It reduces heat generation on the chip and ensures high power efficiency by allowing direct energy transfer from battery supply to output.

III. NON-LINEAR DIGITAL PWM CONTROLLER

In order to fulfill the multi-channel high data rate architecture of the transmitter, a non-linear PWM controller is proposed to generate a pulse signal with variable pulse-width which is used as input signal of the HV transducer driver. The switching power stage for the HV transducer driver is controlled by the non-linear PWM, which selects the operating mode of the power stage based on the input signal magnitude and linearizes the transfer function. The non-linear transfer function from input to duty cycle of the PWM signal has been

derived to linearize the overall transfer function from input to output. The non-linear PWM is realized in digital circuit and its block diagram is illustrated in Fig. 3. The proposed PWM controller consists of S2P converter, data assign block, a MDC, LPWM and noise shaper, pulse generator and clock generator.

S2P converter first converts series-in data to parallel data. Then the input data are assigned to either lookup table register or MDC block based on the pattern of the 16-bit input data by data assign block. The MDC processes the input signal and generates the duty cycle signal and operating mode signal. The operating mode and the duty cycle of the PWM controller are determined based on the magnitude of the 10-bit input data of the MDC. The mode signal is used by the following two blocks to detect the operating mode changing and trigger the different operating logics for the two modes. LPWM and noise shaper compensate the non-linearity of the digital PWM controller caused by the sampling nature of the input signal. Furthermore, the noise shaper is employed to reduce the number of bits of the duty cycle signal to reduce the clock

frequency required by the following pulse generator block. Finally, the bu_pwm and bo_pwm PWM signals are generated by pulse generator.

The bu_pwm and bo_pwm for the buck power stage and the boost power stage are generated independently. Thus, the proposed buck-boost converter has both buck operating mode and the boost operating mode. Those two operating mode power stages share the same inductor and do not need large decoupling capacitor. Hence, this approach requires much less off-chip components as compared to the boost converter with Class-D amplifier design, which can be translated to smaller PCB board area and cheaper price.

A. Boost-Mode Operation

For boost operation, the non-linear PWM modulator is designed as:

$$d = 1 - \frac{V_{BAT}}{v_{in} \cdot G} \tag{1}$$

where G is the DC gain from vin to vout (i.e., G = VOUT/VIN). Hence, the small-signal transfer function from input signal to duty cycle is expressed as:

$$\frac{\hat{d}}{\hat{v}_{in}} = \frac{V_{BAT}}{V_{IN}^2 \cdot G} = \frac{V_{BAT}}{V_{IN} \cdot V_{OUT}} \tag{2}$$

B. Buck-Mode Operation

For buck operation, the non-linear PWM modulator is designed as:

$$d = v_{in} \cdot G / V_{BAT} \tag{3}$$

Therefore, the small-signal transfer function from input signal to duty cycle is expressed as:

$$\frac{\hat{d}}{\hat{v}_{in}} = \frac{G}{V_{BAT}} \tag{4}$$

The expression derived in (1)-(4) are simplified without considering the parasitic components, such like the inductor equivalent series resistance, capacitor equivalent series resistance and the on-resistance of the power transistor. This is to simplify the explanation. With the consideration of these parasitic components, slightly different transfer function equations can be derived, but the idea of the proposed circuit structure, the non-linear pulse-width modulator should be still valid and applicable.

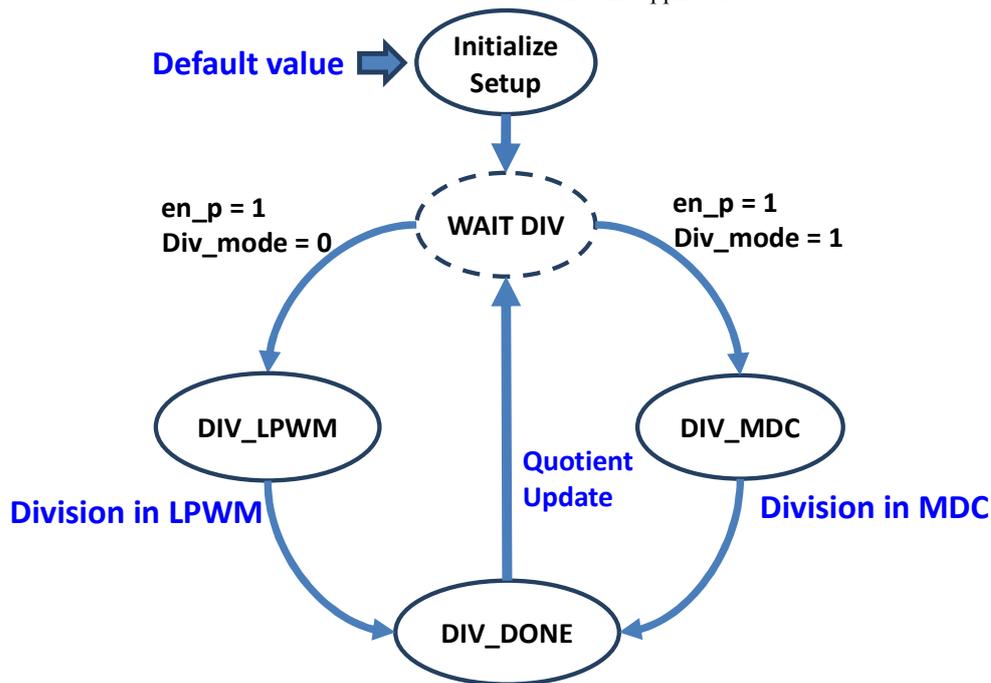


Fig. 4 State diagram of divider controller of digital PWM controller

IV. HARDWARE IMPLEMENTATION AND VALIDATION RESULTS

The implementation system of the proposed PWM controller consists of S2P converter, data assign block, a MDC, LPWM and noise shaper, pulse generator and clock generator. In the expression of buck and boost operating mode and PWM, more than one division calculations are required. It

makes high bit-width divider to be one of the largest hardware resources consumption blocks. Thus, to minimize the chip area, one divider reuse controller is implemented. With the control scheme of the repetitive division operation, only one 20 bits divider is employed to support different division calculation in the system.

A. State Machine of Divider Controller

In order to achieve the optimized design, a controller is introduced to control the input and output of the divider in the proposed PWM controller. As shown in Fig. 4, a state machine based strategy is employed to implement the control algorithm in this controller. In this design, the mealy finite state machine (FSM) includes 5 states.

After RESET signal, default value will be assigned to divider controller during the initial setup state. The divider controller will be in the "WAIT_DIV" state after the initial setup. Then system enable signal "en_p" is monitored and the division cycle starts upon receiving "en_p" signal. Two division cycles are employed here which represent division operation in MDC and division operation in LPWM. These two division cycles are conducted alternatively, which is controlled by the "DIV_MODE" register.

B. Simulation Results

The proposed PWM controller is designed at register-transfer level (RTL) code in Verilog hardware description language (HDL) code and its functions are verified in Simvision. Fig. 5 shows the critical signal simulation waveforms of the proposed digital non-linear PWM controlled buck-boost DC-DC converter.

In this demonstration, a sine signal is employed to be the input test signal. The frequency of the modulating signal is 600 Hz and the modulation index of the PWM signal is 0.9. As illustrated in Fig. 5, the amplified output signal has a swing of 72 V when the PWM signal is applied at the input of the driver. The duty ratio of the pulse-width signal updates as the variation of the input sine signal. This result verified that the buck-boost DC-DC converter works well with pulse-width signals.

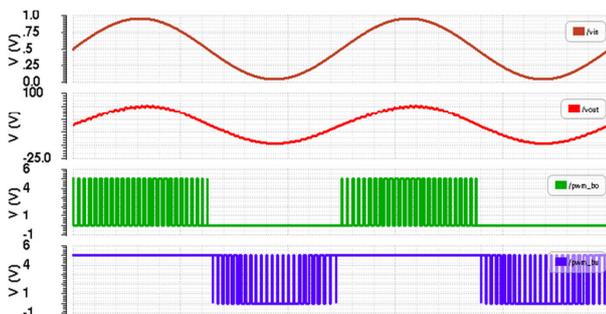


Fig. 5 Signal waveforms of the proposed digital non-linear PWM controlled buck-boost DC-DC converter

C. Hardware Implementation

This controller was then synthesized to gate level netlist, and finally implemented in 1.0 μ m SOI CMOS process. In the final full-chip design of the buck-boost DC-DC converter ASIC system the digital chip core is integrated as a digital macro with analogue blocks. The layout and bonding diagram of the chip are shown in Fig. 6. The layout area of the PWM controller is 2.7 mm \times 2.0 mm. The logic gate count of digital block is about 4K. From the implementation report, with the divider reuse scheme of the repetitive division operation and

other design optimization strategy, more than one third of the total area was reduced.

In this digital control system, to achieve low power consumption, several power saving techniques are applied in implementation. With 1 MHz operating clock frequency, the leakage power is 50% lower than the original design because of the area consumption reduction. In addition, a power reduction of up to 43% of total power consumption is achieved by employing clock gating and operand technology.

V. CONCLUSION

In this paper, a digital non-linear PWM controller in a HV buck-boost DC-DC converter for the piezoelectric transducer of the down-hole acoustic telemetry system is presented. This design is able to work under high temperature and control the generation of output signal with voltage higher than the supply voltage. The proposed PWM controller consists of S2P converter, data assign block, clock generator, a MDC, LPWM and noise shaper and pulse generator. This design is fabricated with the 1.0- μ m SOI CMOS process, which improve the reliability of circuit operation at higher temperature. The implementation results show that the proposed design has the advantages of smaller size, lower power consumption and robust thermal stability.

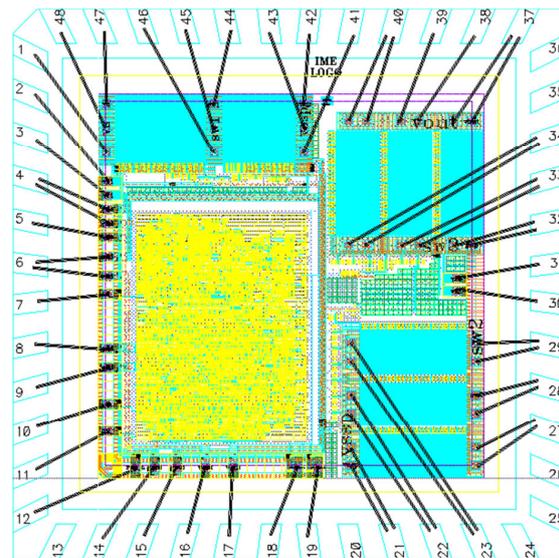


Fig. 6 Layout and bonding diagram of the proposed PWM controlled buck-boost DC-DC converter

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