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Field Programmable Gate Array Based Infinite Impulse Response Filter Using Multipliers

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Abstract**—**In this paper, an Infinite Impulse Response (IIR) filter has been designed and simulated on an Field Programmable Gate Arrays (FPGA). The implementation is based on Multiply Add and Accumulate (MAC) algorithm which uses multiply operations for design implementation. Parallel Pipelined structure is used to implement the proposed IIR Filter taking optimal advantage of the look up table of target device. The designed filter has been synthesized on Digital Signal Processor (DSP) slice based FPGA to perform multiplier function of MAC unit. The DSP slices are useful to enhance the speed performance. The proposed design is simulated with Matlab, synthesized with Xilinx Synthesis Tool, and implemented on FPGA devices. The Virtex 5 FPGA based design can operate at an estimated frequency of 81.5 MHz as compared to 40.5 MHz in case of Spartan 3 ADSP based design. The Virtex 5 based implementation also consumes less slices and slice flip flops of target FPGA in comparison to Spartan 3 ADSP based implementation to provide cost effective solution for signal processing applications.

Keywords**—**Butterworth, DSP, IIR, MAC, FPGA.

I. Introduction

A great part of digital technology deals with digital signal processing. This aspect in engineering has gained increasing interest, especially with much of the world now turning to wireless technology. FPGAs are essentially arrays of uncommitted logic and signal processing resources [1]. These allow the designer to implement DSP functions using highly scalable, parallel processing techniques. There is a constant requirement for efficient use of FPGA resources where for a given system occupying less hardware can yield significant cost-related benefits like reduced power consumption, area for additional application functionality, potential to use a smaller, cheaper FPGA. Today's consumer electronics such as cellular phones and other multi-media and wireless devices often require digital signal processing (DSP) algorithms for several crucial operations in order to increase speed, reduce area and power consumption. Due to a growing demand for such complex DSP applications, high performance, low-cost Soc implementations of DSP algorithms are receiving increased attention among researchers and design engineers. Although ASICs and DSP chips have been the traditional solution for high performance applications, now the technology and the market demands are looking for changes [2]-[5].

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Most of the common functions performed by almost all DSP chips are FFTs, FIR filters, IIR Filters. FIR and IIR digital filters are common DSP functions and are widely used in FPGA implementations. If very high sampling rates are required, fully parallel pipelined architecture must be used [6] where every clock edge feeds a new input sample and produces a new output sample. In case fully parallel implementation is not possible then partly serial approach can be adopted to enhance the system performance which is presented in this paper. Such filters can be implemented on FPGAs using combinations of the general purpose logic fabric, on-board RAM and embedded arithmetic hardware like multipliers and DSP slices. Full-parallel filters cannot share hardware over multiple clock cycles and so tend to occupy large amounts of resource. Hence, efficient implementation of such filters is important to minimize hardware requirement. When implementing a DSP system on a platform containing dedicated arithmetic blocks, it is normal practice to utilize such blocks as far as possible in reference to any general purpose logic fabric. On one hand, high development costs and time-to-market factors associated with ASICs can be prohibitive for certain applications while, programmable DSP processors can be unable to meet desired performance due to their sequential-execution architecture. In this context, embedded FPGAs offer a very attractive solution that balance high flexibility, time-to-market, cost and performance [7]. Therefore, in this paper, an IIR filter is designed and implemented on FPGA. The new generations of FPGA not only provide an effective way of implementing high performance DSP functions but also provide the designer with an even more cost-effective solution.

II. IIR Filter

Digital filter design is the process to derive the transfer function H (z). There are two possibilities of deriving digital filters e.g. Infinite Impulse Response or Finite Impulse Response. Recursive filters are the efficient way of achieving a long impulse response, without having to perform a long convolution. They have less performance flexibility than other digital filters but execute very rapidly and these filters are also called Infinite Impulse Response (IIR) filters [8]-[10], since their impulse responses are composed of decaying exponentials [11]. This distinguishes them from digital filters which are being carried out by convolution, called Finite Impulse Response (FIR) filters. Infinite Impulse Response convert the digital filter specifications into an analog prototype low pass filter specifications. It can determine the analog low pass filter transfer function $H_a(s)$ meeting the

specifications and can transform $H_a(s)$ into the desired digital transfer function H(z) [12].

This approach has been widely used for the following reasons, firstly the advanced approximation techniques are highly advanced and they usually yield closed form solutions. Secondly, extensive tables are available for analog filter design and many applications require digital simulation of analog systems. The conversion of $H_a(s)$ into H(z) includes mapping from the s-domain to the z- domain so that essential properties of the analog frequency response are preserved. Thus, the mapping should be in such a way that the imaginary axis in the s- plane (jΩ) be mapped into the unit circle of the z-plane and a stable analog transfer function be mapped into a stable digital transfer function [13], [14]. The transfer function of an IIR filter can be expressed as:

$$H(z) = \frac{B(z)}{A(z)} = \frac{\sum_{m=0}^{N} b_n z^{-m}}{\sum_{n=0}^{N} a_n z^{-n}} \quad (1)$$

It can be written as:

$$H(z) = \frac{b_0 + b_1 z^{-1} + \ldots\ldots b_n z^{-M}}{a_0 + a_1 z^{-1} + \ldots\ldots a_N z^{-N}}, \; a_0 = 1 \quad (2)$$

Bilinear transform can be used for s plane to z plane mapping by using:

$$S = \frac{2}{T}\left(\frac{1 - z^{-1}}{1 + z^{-1}}\right) \quad (3)$$

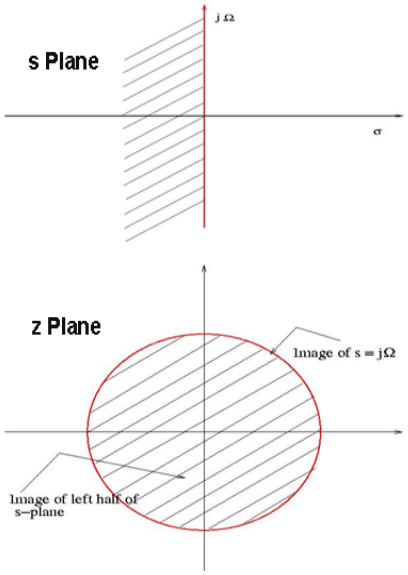

Fig. 1 s plane to z plane mapping

This transformation maps a single point in the s- plane to a unique point in the z- plane and vice –versa as shown in Fig. 1.

III. Proposed Design Simulation

In this section, Direct Form II based low pass Butterworth IIR filter has been designed and simulated using Matlab [15]. When the ripple is set to 0%, the filter is called a maximally flat or Butterworth filter. The Magnitude squared frequency response of N^{th} order low pass Butterworth filter is:

$$|H_a(\Omega)|^2 = \frac{1}{1 + (\Omega / \Omega_c)^{2N}} \quad (4)$$

$$= \frac{1}{1 + e^2(\Omega / \Omega_p)^{2N}} \quad (5)$$

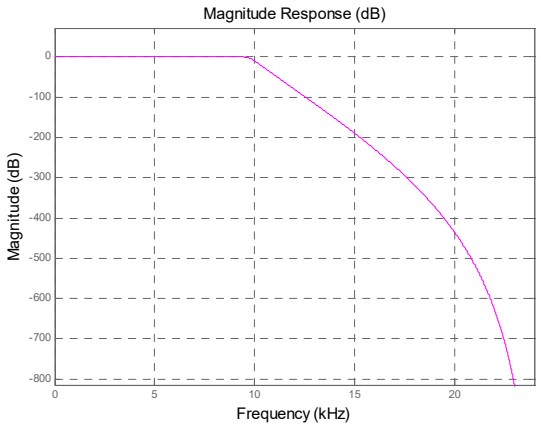

Fig. 2 IIR Magnitude Response

An IIR filter of order 31 has been achieved by taking pass edge frequency of 0.4, stop edge frequency of 0.5, pass band ripples of 1 db and stopband attenuation of 80 db. The magnitude response of designed filter has been shown in Fig. 2. Its equivalent impulse response and step response has been shown in Figs. 3 and 4 respectively.

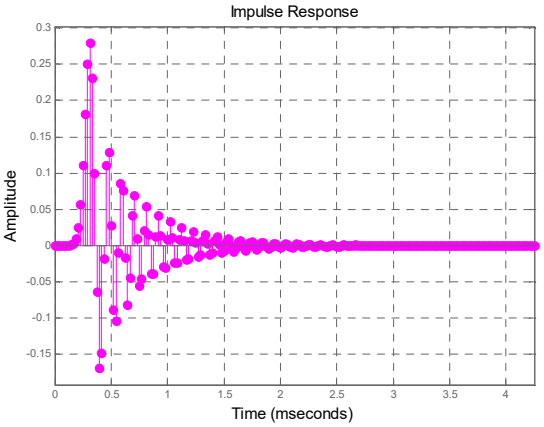

Fig. 3 IIR Impulse Response

Its equivalent pole/zero response is shown in Fig. 5.

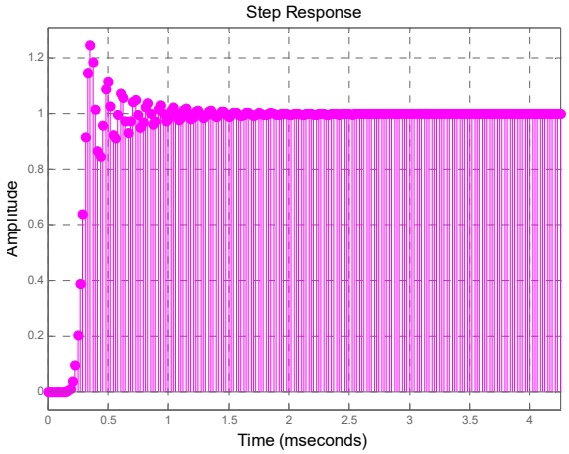

Fig. 4 IIR Step Response

IV. Hardware Synthesis

In this section, VHDL code of the simulated IIR filter has been designed and implemented using MAC algorithm. The DSP 48E and DSP 48 slice based FPGAs are used to perform the multiplier function. The modelsim based simulated response of IIR filter has been shown in Fig. 6.

The hardware implementation of IIR filter includes embedded DSP slices and pipelined registers to enhance the speed performance. The proposed MAC based FIR filter structure is shown in Fig. 7.

Fig. 5 IIR Pole Zero Response

To observe the speed and resource utilization, the developed IIR filter has been synthesized on Virtex 5 based xc5vlx330 FPGA and Spartan 3DSP based xc3sd1800 FPGA.

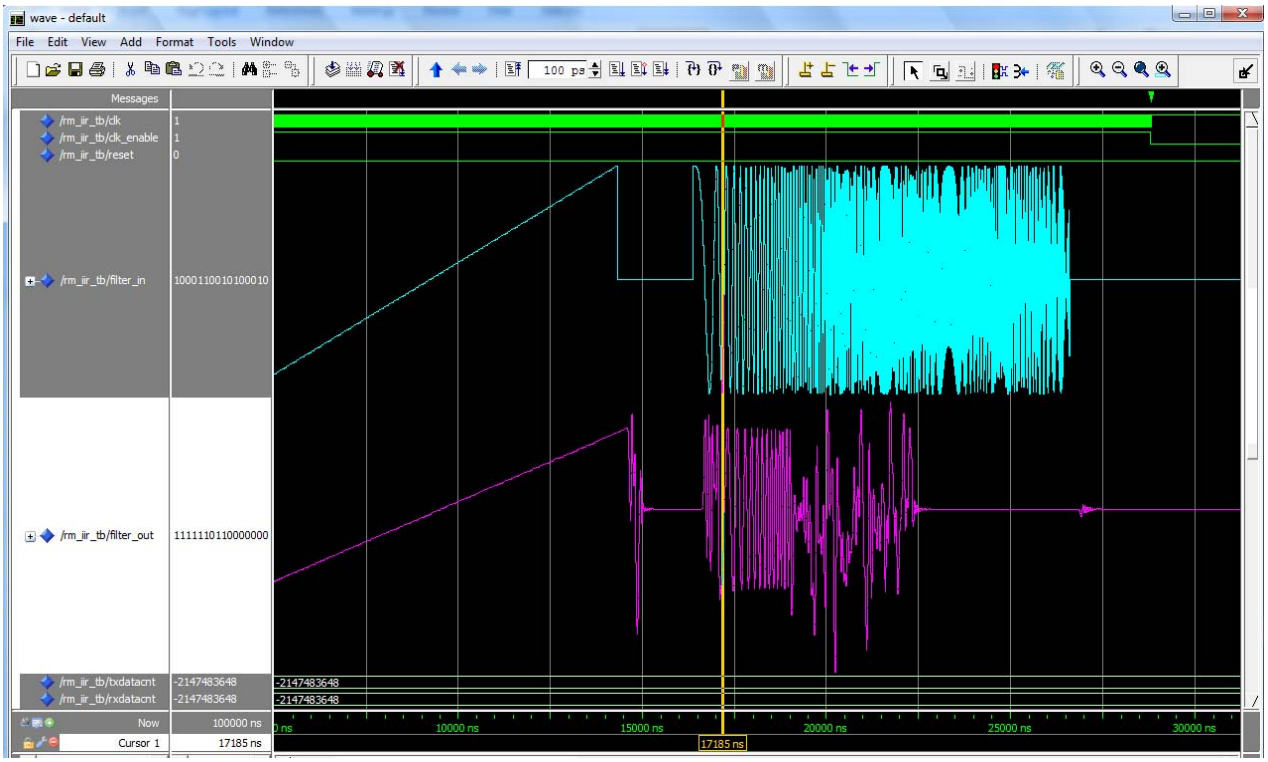

Fig. 6 Modelsim Based IIR Response

The resource utilization and speed performance on both FPGAs are compared and analyzed. The Virtex 5 based design can operate at an estimated frequency of 81.5 MHz as compared to 40.1 MHz in case of Spartan 3 ADSP based design.

The resource utilization on both devices is shown in Tables I and II.

TABLE I
RESOURCE UTILIZATION ON VIRTEX 5

Sr. No	Logic Details	Used/Available	Utilization (%)
1.	Number of Slices	750/207360	0
2.	Number of Flip Flops	248/3192	7
3.	Number of LUTs	2690207360	1
4.	Number of IOBs	35/1200	2
5.	Number of DSP 48Es	47/192	24

It can be observed from Table III that Virtex 5 based design consumes less resources in terms of slices and slice flip flops.

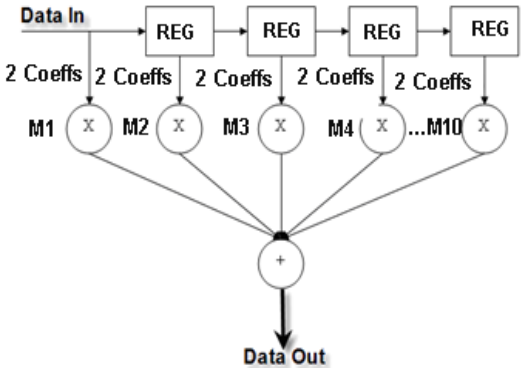

Fig. 7 MAC Based IIR Filter

TABLE II
RESOURCE UTILIZATION ON SPARTAN 3 ADSP

Sr. No	Logic Details	Used/Available	Utilization (%)
1.	Number of Slices	1556/16640	9
2.	Number of Flip Flops	509/33280	1
3.	Number of LUTs	2690/33280	8
4.	Number of IOBs	35/309	11
5.	Number of DSP 48s	47/84	55

TABLE III
RESOURCE UTILIZATION COMPARISON

Sr. No	Logic Details	Spartan 3 ADSP	Virtex 5
1.	Number of Slices	1556	750
2.	Number of Flip Flops	509	248
3.	Number of LUTs	2690	2690
4.	Number of IOBs	35	35
5.	Number of DSP 48s	47	47

V. CONCLUSIONS

In this paper, a MAC algorithm pipelined architecture for IIR filter has been presented to enhance the speed and reduce the area consumption by taking an optimal advantage of look up table and embedded DSP slices of target FPGAs. The proposed filter has been designed and simulated using Matlab. The developed design has been synthesized on Virtex 5 based xc5vlx330 FPGA and Spartan 3DSP based xc3sd1800 FPGA. The result shows that the Virtex 5 based IIR filter can operate at almost double estimated frequency as compared Spartan 3 ADSP based design. The resource consumption of Virtex 5 based design is less as compared to other in terms of slices and flip flops.

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