International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:8, No:1, 2014

Design of CMOS CFOA Based on Pseudo Operational Transconductance Amplifier

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Abstract**—**A novel design technique employing CMOS Current Feedback Operational Amplifier (CFOA) is presented. The feature of consumption very low power in designing pseudo-OTA is used to decreasing the total power consumption of the proposed CFOA. This design approach applies pseudo-OTA as input stage cascaded with buffer stage. Moreover, the DC input offset voltage and harmonic distortion (HD) of the proposed CFOA are very low values compared with the conventional CMOS CFOA due to the symmetrical input stage. P-Spice simulation results are obtained using 0.18μm MIETEC CMOS process parameters and supply voltage of ±1.2V, 50μA biasing current. The p-spice simulation shows excellent improvement of the proposed CFOA over existing CMOS CFOA. Some of these performance parameters, for example, are DC gain of 62. dB, open-loop gain bandwidth product of 108 MHz, slew rate (SR+) of +71.2V/μS, THD of -63dB and DC consumption power (P_C) of 2mW.

Keywords**—**Pseudo-OTA used CMOS CFOA, low power CFOA, high-performance CFOA, novel CFOA.

I. Introduction

IN recent years, great interest has been devoted to the analysis and design of current feedback op-amp and current-conveyor integrated circuits, mainly because these circuits exhibits better performance, have particularly higher speed and better bandwidth than classic voltage-mode operational amplifiers (VOA) [1]. However, the conventional CMOS CFOA design is still facing certain problems, first, the offset voltage on the current feedback cannot be made zero. CFOA usually adopts an analog buffer as the input stage. As a result, the non-inverting input has very high impedance while the inverting input has very low impedance. Hence, the CFOAs offset is higher than folded cascade voltage amplifier (VFA) Design. Second, the constant bandwidth feature of the CFOA is only approximate if the inverting input impedance is not small enough [2], [3]. The low–voltage and low power consumption are considered as an important aspect of the performance of an amplifier especially when signals are in the range of few hundred microvolts [4]. Several low voltages, low power CMOS realizations for the CFOA have been reported in the literature [5]-[12]. The design still suffers from many drawbacks such as high distortion, high noise, and complex circuitry. The CFOA has been always seen as an extension of the CCII; therefore, the design approach was cascade with CCII+ with a voltage follower to realize a complete circuit. The obtained bandwidth was always the degraded version of CCII+. The current feedback operational amplifier (CFOA) is a two-port (four-terminal) network. The CFOA could be realized by using second generation current conveyor CCII+ cascaded with a voltage follower [13].

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This paper describes a novel design of CMOS CFOA design which provides high symmetrical impedances (infinite for DC) inputs together with low power consumption (PC) low supply voltage. This design approach applies fully differential pseudo-OTA as input stage cascaded with class AB cross coupled buffer stage. The symmetrical input stage of pseudo-OTA is reducing the DC offset voltage and power consumption of CMOS CFOA with the improvement of high-frequency parameters. Moreover, class AB cross coupled buffer stage provides high current drive capability. P-Spice simulation results confirm the theoretical calculations.

II. Theoretical Background of Pseudo-OTA

Fully-differential OTA is typical pair with the tail current source, and pseudo-differential is based on two independent inverters without a tail current source as shown in Fig. 1 avoiding the voltage drop across the tail current source in a PD structure allows achieving wider input range and makes the architecture attractive for low voltage applications. Removing the tail current source, however, results in larger common-mode gain (ACM). In an FD structure, the common-mode gain can be reduced by increasing the output resistance of the bias current source. However, for the pseudo-OTA shown in Fig. 1, Common Mode (CM) voltage gain is equal to the differential mode (DM) voltage gain (= gm R_0), i.e., CMRR= DM=CM=1. This large CM, in pseudo-differential structures, can lead to huge common-mode variations at the OTA outputs unless a fast and strong CMFB is used [14].

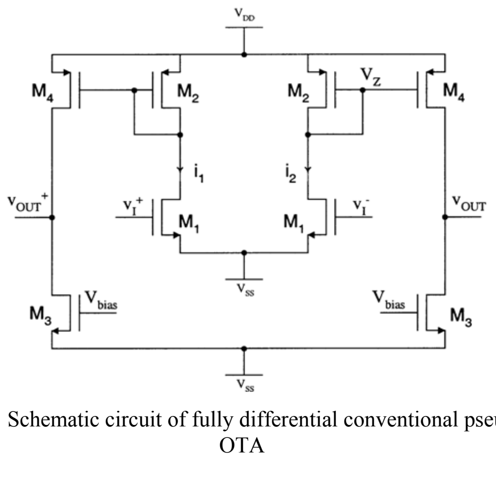

Fig. 1 Schematic circuit of fully differential conventional pseudo-OTA

International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:8, No:1, 2014

Using a balanced configuration with two single-ended transconductances reduces ACM at low frequency to the order of unity. This approach adds more load to the driving stage due to the connection two input transistors, thus doubling the input capacitance. The same also applies to the case of the common-mode feed forward (CMFF) technique. A common-mode gain, at low frequency, is given by [14]:

$$A_{CM} = \frac{v_{ocm}}{v_{icm}} = \frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \cong \frac{g_{m1}}{g_{m2}} \quad (1)$$

The operation of pseudo-OTA consists of one differential pair consisting of NMOS transistors M_1 and M_2.MOS transistors M_3 and M_4 provide the DC bias. The pseudo-OTA characterized by performance such as high DC voltage gain, wide gain bandwidth product, low noise and consumption power [15]. The gain of the pseudo-OTA is given by:

$$V_O/V_{in} = G_{m1} R_O \quad (2)$$

and the gain bandwidth product is given by:

$$GBW = G_{m1}/C_L \quad (3)$$

where G_{m1} is the transconductance of transistor M_1 and R_O(output resistance) =(R_O looking into the drain of M_3)//(R looking into transistor into the drain of M_4). After applying the design strategy clarified previously, the design parameters in strong inversion region, the gate-dimensions, and biasing currents, of MOS transistors are summarized in Table I.

TABLE I
GATE DIMENSIONS AND BIASING CURRENTS OF MOS TRANSISTORS OF PROPOSED CMOS CFOA

Transistors no.	Gate dimensions and biasing currents		
	W(μm)	L(μm)	Biasing Current(μA)
M_1	12.0	0.18	25
M_2	16.1	0.18	25
M_4	11.59	0.18	50
M_3	6.21	0.18	50
M_6	9.5	0.35	50
M_5	2.0	0.18	50
M_7	23.8	0.18	50
M_8	6.0	0.18	50

In our proposed CFOA using feedback technique of pseudo-OTA by connecting the positive output terminal to the negative input terminal as shown in block diagram of Fig. 2. This technique called current feedback OTA technique [16]. This approach represents input stage of proposed CFOA and cascading with buffer stage as shown in the schematic circuit of Fig. 3.

III. Simulation Results

A new alternative CMOS CFOA with the high-performance operation, very low input offset voltage, and low distortion are proposed in this paper. Since, the high-frequency parameters such as voltage gain, (–3dB) bandwidth, slew rate (SR), settling time (ts) and gain bandwidth product (GBW) are improved. Fig. 3 clarifies the improvement in the open loop voltage gain and gain bandwidth product (GBW) of the proposed CMOS CFOA. Also, the magnitude curve in Fig. 4 shows the frequency response (variation of frequency against the voltage gain and phase curve shows the variation of frequency against the phase shift between input and output voltage.

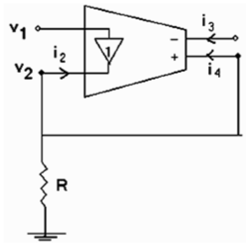

Fig. 2 Block Diagram of current feedback pseudo-OTA

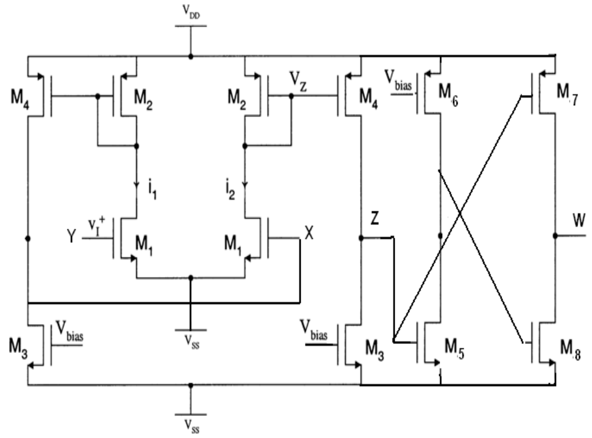

Fig. 3 Schematic circuit of proposed CFOA based on pseudo-OTA

The value of output impedance of buffer stage is decreased drastically due to using cross-coupled buffer stage. Fig. 5 indicate that the improvement in closed loop (-dB bandwidth) of the proposed CMOS CFOA, since the values of (-dB bandwidth) is 108 MHz compared with 46.2MHz with introduce the closed loop resistors are R_F=1KΩ and R_I=1KΩ. The value of voltage gain will increase with decreasing in the (-3db) bandwidth due to change the value of R_I and keep the value of R_F is constant. The slow rate of CMOS and CFOA are measured from Fig. 6. DC characteristics of CMOS CFOA is shown in Fig. 7, we note that there is a large enhancement in linearity of DC characteristics of the CMOS CFOA due to the symmetry in the operation of the fully differential input stage of the pseudo-CFA OTA. Moreover, we note that the value of input offset voltage is -0.1mV due to the symmetry in the input stage (inverting and non-inverting inputs) of the proposed CMOS CFOA. Table II shows the effect of varies input resistors R_I value on the feedback loop gain and CMOS CFOA, closed loop voltage gain (Av), gain bandwidth product

(GBW), (-3dB) bandwidth, phase margin(PM), and total harmonic distortion(HD). Simulation results of proposed CMOS CFOA confirmed the theoretical concepts in previous sections.

TABLE II
PERFORMANCE PARAMETERS OF THE PROPOSED CMOS CFOA AS INPUT RESISTOR (R_I) IS VARIED

R_I KΩ	-3dB B.W MHz	GBW MHz	PM deg.	THD dB	Av dB
1	79.6	108	49.9°	-67.0	5.9
0.3	32.7	89.2	48.6°	-65.0	12.5
0.1	10.7	81.8	46.0°	-41.7	20.4
0.01	1.0	78.6	45.0°	-41.0	39.1

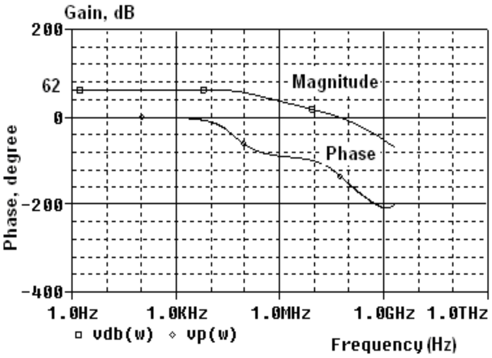

Fig. 4 Open-loop frequency response of the proposed CMOS CFOA

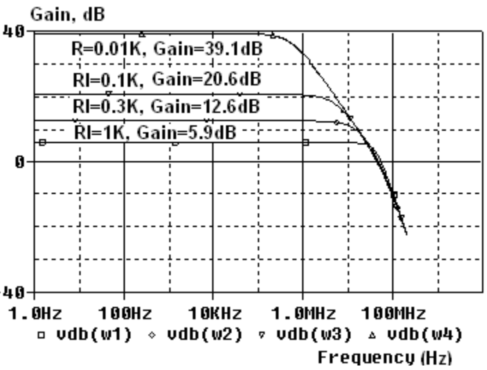

Fig. 5 Closed-loop frequency response of the proposed CMOS CFOA as R_I is varied from 0.01KΩ to 1 KΩ

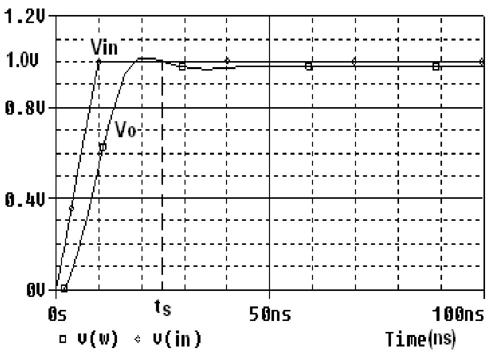

Fig. 6 Transient response of the proposed CMOS CFOA

TABLE III
SUMMARIZED PERFORMANCE PARAMETERS OF THE PROPOSED CMOS AND CFOA

Parameters	CMOS CFOA
Supply voltage	±1.2
Biasing current	50µA
Open loop gain @R_L=10KΩ, C_L=10p	62.0dB
Open loop (GBW) at RL=10KΩ, C_L=10pF	108MHz
Compensation capacitor (Cc)	0.5pF
Phase Margin (PM)	53°
Trans impedance gain at node (Z)	156dB
Closed loop (GBW) @R_F = 1KΩ, R_I = 1KΩ	46.2MHz
Phase Margin (PM)	80°
Slew rate @ C_L=10p	+71.2 V/µS, -61V/µS
Settling time@ C_L=10p	46.0 ns
Total harmonic distortion(THD)	-63.0 dB
Input offset voltage @Vin=0V	-0.1mV, 0.15 mV
Consumption power	2.0 mW
Die area	0.052 mm^2

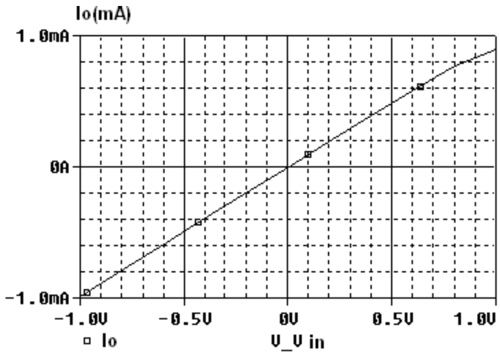

Fig. 7 DC characteristics of the proposed CMOS CFOA

IV. CONCLUSION

A new design technique of the CMOS CFOA with attractive features for high frequency, low offset voltage, and low distortion is proposed in this paper. The proposed design based on cross-coupled buffer stage that connected as the output stage of the CMOS CFOA. Since this technique operates on logic transition concept that gives the high speed, symmetry operation of the output signal and high current drive capability of proposed CMO CFOA. The high speed operation improved high performance parameters such as gain bandwidth (GBW), (-3dB) bandwidth, slew rate (SR) and settling time (t_s) with ensure the phase margin (PM) in acceptable value that keep the stability of operation. Moreover, the symmetry of input differential of pseudo-CFA OTA technique decreased the distortion in the output signal and improved (DC) characteristics of CMOS CFOA. Also to that using pseudo-OTA as the input stage of CMOS CFOA make the symmetry of inverting and non-inverting inputs that reduce input offset voltage. The trans-impedance node (Z) of the CMOS CFOA gained high value due to cascading transistors of CFA OTA. This feature is very important for design CMOS CFOA with high gain. We can summarize our conclusion by saying that the proposed CMOS CFOA with symmetry of the input stage and symmetry of the output stage will gain CMOS CFOA attractive features for many high frequencies, low distortion, low input offset voltage applications. Also, the CMFB circuit is avoided due to the connection of the output terminal of the pseudo-OTA to input terminal to propose current feedback OTA.

REFERENCES

[1] Ahmed H. Madian, Soliman A. Mahmoud, and Ahmed M. Soliman, "New 1.5-V CMOS Current Feedback Operational Amplifier", IEEE, 2006, pp. 600-603.
[2] Salvatore Pennisi, "High-Performance CMOS Current Feedback Operational Amplifier", IEEE Journal, 2005, pp. 1573- 1576.
[3] Hio Leong Chao and Dongsheng Ma, "CMOS Variable-Gain Wide-Bandwidth CMFB-Free Differential Current Feedback Amplifier for Ultrasound Diagnostic Applications", IEEE Journal, 2006, pp. 649-652,
[4] G. Giustolisi, G. Palmisano, G. Palumbo and S.Pennisi, "High-Drive CMOS Current-Feedback Opamp", IEEE Journal, 1997, pp. 229-232
[5] Jirayuth Mahattanakul and Chris Toumazou, "A Theoretical Study of the Stability of High-Frequency Current Feedback Op-Amp Integrators", IEEE Transactions on Circuits and Systems, vol. 43, no.1, January 1996, pp. 1-12.
[6] Giuseppe Di Cataldo, Alfio Dario Grasso and Salvatore Pennisi, "Two CMOS Current Feedback Operational Amplifiers", IEEE Transactions on Circuits and Systems, 2007, pp. 1-5.
[7] Ali Assi, Mohamad Sawan, and Jieyan Zhu, "An offset compensated and High- Gain CMOS Current-Feedback Op-Amp", IEEE Transaction on Circuits and Systems, vol. 45, no. 1, January 1998. pp. 85-90.
[8] Aly M. Ismail and Ahmed M. Soliman, "Novel CMOS Current Feedback Op-Amp Realization Suitable for High-Frequency Applications",", IEEE Transaction on Circuits and Systems, vol. 47, no. 6, June 2000, pp. 918-921.
[9] S. Selvanayagam and F. J. Lidgey," Wide Bandwidth CMOS Current Feedback Op Amp for Inverting Applications", IEE Electronics Letters Journal, 1998, pp. 1-4.
[10] Jieyan Zhu, Mohamad Sawan, and Karim Arabi, "An Offset Compensated CMOS Current-Feedback Operational Amplifier", IEEE Journal, 1995, pp. 1552-1555.
[11] G. Palumbo and S. Pennisi, "Current-Feedback Amplifiers versus Voltage Operational Amplifiers", IEEE Transaction on Circuits and Systems, vol. 48, no.5, May 2001. pp. 617-623.
[12] M. Djebbi, A. Assi and M. Sawan, "An Offset-Compensated Wide-Bandwidth CMOS Current-Feedback Operational Amplifier", IEEE Journal, 2003, pp. 73-76.
[13] Soliman A. Mahmoud, Ahmed H. Madian, and Ahmed M. Soliman, "Low- voltage CMOS current Feedback Operational Amplifier and its Applications", pp. 212-218 ETRI Journal, vol. 29, no. 2, April 2007, pp. 655-658.
[14] Ahmed Nader Mohieldin, Edgar Sánchez-Sinencio, and José Silva-Martínez, "Nonlinear Effects in Pseudo-Differential OTAsWith CMFB", IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, vol. 50, no. 10, October 2003, pp. 762-770.
[15] Phillip E. Allen and Douglas R Holberg, CMOS Analog circuit design, second edition, New York Oxford University Press, 2004.
[16] Hanspeter Schmid, "The Current-Feedback OTA", IEEE Journal, 2001, pp.655-658.