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Design of an Efficient Retimed CIC Compensation Filter

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***Abstract*—**Unwanted side effects because of spectral aliasing and spectral imaging during signal processing would be the major concern over the sampling rate alteration. Multirate-multistage implementation of digital filter could come about a large computational saving than single rate filter suitable for sample rate conversion. This implementation can further improve through high-level architectural transformation in circuit level. Reallocating registers and relocating flip-flops across logic gates through retiming certainly a prominent sequential transformation technology, that optimize hardware circuits to achieve faster clocking speed without affecting the functionality. In this paper, we proposed an efficient compensated cascade Integrator comb (CIC) decimation filter structure that analyze the consequence of filter order variation which has a retimed FIR filter being compensator while using the cutset retiming technique and achieved an improvement in the passband droop by 14% to 39%, in computation time by 38.04%, 25.78%, 12.21%, 6.69% and 4.44% and reduction in path delay by 62.27%, 72%, 86.63%, 91.56% and 94.42% of 3, 6, 8, 12 and 24 order filter respectively than the non-retimed CIC compensation filter.

***Keywords*—**Multirate Filtering, CIC decimation filter, Compensation theory, Retiming, Retiming algorithm, Filter order, Synchronous dataflow graph.

I. Introduction

HIGH data-rate communication systems have enormous real-time computational requirements. A modern cellular phone, for example, executes several complex algorithms, including speech compression and decompression, highly complex modulation and demodulation, upconversion and down-conversion of modulated and received signals, and so forth. Multirate processing is essentially a powerful technique that substantial loss of computational complexity by changing the sampling frequency of any input digitally. The important role of multirate filtering is to enable the sampling rate conversion in the digital signal without significantly destroying the signal components of interest. The rapid growth and development of the new algorithms and new design methods has been influenced through the advanced technology. High-speed, low area and low power consumption would be the three constraints of these algorithms for implementing the design.

Multirate digital signal processing deals with the sampling rate conversion of a digital signal, including decimation and interpolation. An effective way of enhancing the efficiency of filter designs is to use several stages connected in cascade (series) by which, first stage addresses the narrow transition band without requiring an increased implementation cost and subsequent stages make-up for compromises for making the first stage to be efficient. The design process needs to explore competing design objectives for instance speed, area, power, timing and many others. Several mathematical transformations and algorithms help to keep these design perspectives and also the defined requirement specifications, transformations are applied that trade off less relevant design objectives against the other more important objectives.

E. B. Hogenauer [1] suggested a comb based filter often known as cascade Integrator comb (CIC) filter for efficient downsampling or upsampling of any input with sampling rate F_s and which has an immense advantage when aiming for low power consumption because multiplierless structure. This structure is represented in sequentially connected integrator and comb sections designed through adders and delay elements. Retiming is often a traditional sequential optimization technique, initially proposed by Leiserson and Saxe in [2] to reduce the clock period and area of edge-triggered sequential circuits and work towards the principle of lowering the computation time from the critical path (i.e. path using the longest computation time among all paths that have zero delays) in order to decrease power consumption by reducing switching in static CMOS circuit.

Cutset retiming technique is a special class of retiming in which the clock period is reduced by reducing delays on critical nets. This process involves the transferring of quantity of delays such that don't modify the transfer function with the DFG.

G. J. Dolecek et al. [3]-[6] designed an efficient multiplier-free CIC-cosine decimation filter and compensation filter based on the 2N-order filter when using the sharpening technique on the high input rate. It tries to help the pass band and also the stop band of a symmetric nonrecursive FIR filter when using the multiple copies of the filter because nice characteristics, for example linear-phase, stability, robustness to quantization effects, and pipelining. On this process filter order of compensating filter imposes a large impact on its output characteristics, performance and iteration period as well as its hardware complexity and for that reason a trade-off is required to achieve an optimal structure to relieve the circuit complexity and computational time [7]. Gupta P. et al. designed a high-speed implementation of 8th order all pole lattice filters using retiming methodology [8]. V. Zivojnovi et al. presented the retiming of DSP algorithms exhibiting multirate behavior when using the non-ordinary marked graph

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model as well as the reachability theory through the valid retiming condition of multirate graphs [9]. Various methods happen to be introduced to reduce the power consumption as well as to enhance the circuit speed in multirate filtering, which utilizes the non - recursive structure of a comb filter, but the compensation of passband droop and filter order of compensator would be the major concern. Retiming and polyphase implementation of compensator filter made overall sampling rate conversion system considerably faster and cost effective than the original digital down conversion (DDC) system. Kwentus et al. [10] outlined a method which utilizes the sharpening technique to decrease the passband droop in order to enhance the stopband attenuation at higher input rate.

Khoo, K. Y. et al. [11] proposed an effective architecture utilizing a first carry-save integrator stage inside a high-speed CIC decimation filter and achieved a decrease in the quantity of registers by 6.3% to 13.5%. Shih-Hsu Huang et al. presented retiming transformation [12] that relocates registers from the circuit to shorten the time cycle a serious amounts of help the speed constraint further. Cong, J. et al. presented a practical solution for simultaneous retiming and multilevel global placement to optimize the performance using sequential timing analysis. They extend the analysis to deal with gates/clusters with multiple outputs and integrate it right into a multilevel optimization framework for simultaneous retiming and placement [13].

Many researches focused on significant savings of area and power [14]-[16] through minimizing contributions period. Paper [17] presents a multistage CIC-cosine decimation filter with 2N-order compensation filter structure when the cascade of expanded cosine prefilters is included with improved stopband CIC characteristic and compensator structure to compensate low passband droop along with clock period minimization. Recently, in 2012, Pecotic, M.G. et al. [18] presented a worldwide optimization technique depending on the interval analysis for your design of finite-impulse-response CIC compensators whose coefficients are expressed since the sums of powers of two (SPT) using minimax error criterion to reduce the sampling period. Y. Diao et al. presented a simple retiming algorithm integrated with rewiring for flip-flop reductions [19] and Yagain D. et al. created a cutset retiming technique within the synchronous data flow graphs to acquire high-speed digital circuits [20] that can be used for faster sampling rate conversion.

In this proposed work, an efficient approach to design a compensated CIC decimation filter structure using retiming algorithm is described. We analyzed the effect of filter order variation on compensated CIC decimation filter structure with retimed compensator FIR filter along with the improvement in passband droop.

Other paper is organized as follows. Preliminary background of multirate filtering is briefly described in Section II. Section III presents the retiming algorithm as well as different constraints being an efficient transformation technique. Some advance compensation techniques and theory of polyphase implementation is discussed in Section IV. Section V describes the proposed procedure for design CIC decimation filter using retiming algorithm and it is the basic setup. Performance analysis and simulation results of designed retimed compensated CIC decimation filter are mentioned in Section VI. Finally a quick discussion and conclusions are used Section VII.

II. Preliminary Background of Multirate Filtering

Inside a sampled signal, some quantity of excess bandwidth occurs to compensate the aliasing that occurs inside transition band. The Multirate implementation yields a Multirate-multistage design which lowpass filters data while decreasing the sampling rate each and every stage for maximum computational efficiency. In several applications, if a very narrow transition width is required in accordance with the sampling frequency, we lower the sampling rate in stages by utilizing simple lowpass filters with specific order.

The locations of poles and zeros with the digital filters directly depend on the significance of filter order and coefficients. Decimation or interpolation processes modify the worth of poles and zeros therefore, the location of poles and zeros are going to be shifted from your desired location; therefore, this may create deviations from the frequency response on the system.

Decimation and interpolation filters are classified as the key building blocks of a sampling rate conversion system due to its low-pass filtering or over/down-rate sampling capability. Decimation filter (Decimator) converts the lower resolution, high bit-rate data to high quality low pitch data while interpolation filter (interpolator) converts high-resolution, low bit-rate data to low-resolution, high- frequency data furthermore while using the elimination of quantization noise. During this conversion process, down-sampling is afflicted with aliasing whereas up-sampling produces the unwanted spectra within the frequency band appealing, respectively. Hence, decimation has to be performed such that steer clear of the results of aliasing, which occurs when the high frequency within the spectrum of any down-sampled signal w_H exceeds the value π/N.

When constructing a Multirate system for fast decimation process, it's desirable to create an efficient implementation structure using DSP algorithms. Timothy W. O Neil et al. introduced a retiming algorithm in single rate data flow graphs of your digital filter operating on small clock periods to relieve the execution time of synchronous data flow graphs [24]. Xun Liu et al. applied retiming for clock period minimization and tolerance maximization to clock signal delay variation [25]. Obviously, the efficiency on the sampling rate converters using these advance processing algorithms may improve with regard to synchronous data flow output period.

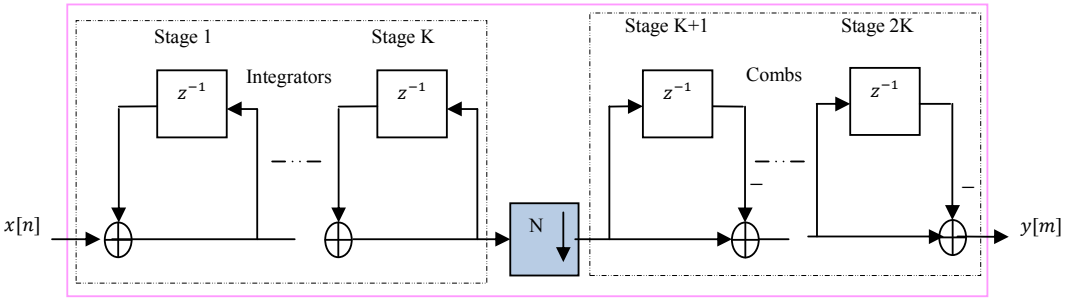

Fig. 1 Block diagram representation of CIC Decimator: Implementation structure consisting of the cascade of K integrators, down sampler, and the cascade of K differentiators

A. Cascade Integrator-Comb (CIC) Filter

Comb filters are a special class of multirate filter which might be implemented without multipliers as a result of unity-valued feedback coefficients. CIC decimation/ interpolation filter is a unique filter structure therein comb group which contains an integrator block working with the oversampled frequency F_s, a clock divider for rate reduction and a block of differentiator working at F_s/k, where k is the decimation ratio. The multiplierless structure of the CIC filter causes it to become an essential component of the first stage of the multistage design as throughout the decimation process, the sampling-minute rates are higher [1]. It becomes an attractor for many hardware such as FPGAs and ASICs because multipliers use up a lot of the region and is particularly hard to make to function at quite high clock rates. Hence, this filter class is suitable for just a single- chip VLSI implementation that can operate at high frequencies.

However, the drawback to a CIC filter could be that the response with the CIC filter provides a poor lowpass characteristic, and that is undesirable in most applications. Fortunately, this problem might be alleviated by way of a compensation filter. In section 4 several techniques are discussed to compensate this passband droop also to increase the lowpass characteristic of the CIC filter during the decimation process. CIC filter structure happen to be constructed by building a pole as well as a zero at $z = 1$. This pole/zero pair should cancel, yielding the traditional FIR transfer function.

The fundamental notion of a comb-based decimator is explained in Fig. 1. The figure shows the factor-of-N Decimator is composed of the K-stage CIC filter plus the factor-of-N down-sampled. The CIC filter first performs the averaging operation, then follows it using the decimation. The transfer function of the CIC filter on z-domain is given in (1):

$$H[z] = H[z]^{K}_{Integrator} \cdot H[z]^{K}_{Comb} = \left[\frac{1}{N}\left(\frac{1-z^{-N}}{1-z^{-1}}\right)\right]^{K}$$
$$= \left[\frac{1}{N}\left(\frac{(1-z^{-1})(1+z^{-1}+\cdots\ldots+z^{-N+1})}{(1-z^{-1})}\right)\right]^{K} = \left[\frac{1}{N}\left(\sum_{p=0}^{N-1} z^{-p}\right)\right]^{K} \quad (1)$$

For decimation with a factor of N, the first data must be in a bandwidth due to $F_s/(2N)$, where F_s could be the rate from which an original data was sampled. Thus, if the original data contains valid information inside the component of the spectrum beyond $F_s/(2N)$, decimation is not possible. CIC decimators are generally designed and implemented through the pipelined structure to ensure high system clock frequencies.

III. Retiming and Cut-Set Retiming

Broadly, signal processing systems are usually classified as feedforward or feedback systems. Many of the signal processing algorithms like fast Fourier transform (FFT) and discrete cosine transform (DCT) are feedforward. The timing may be improved through adding multiple stages of pipelining inside hardware design. A critical path running through a combinational cloud inside a feed forward system may be broken by the addition of pipeline registers. Pipelining and retiming are two different aspects of digital design.

In pipelining, additional registers are added that change the transfer function in the system, whereas in retiming, registers are relocated within a design to optimize the required objective with clock period reduction and unaltered circuit functionality. Implementation of clock management techniques can minimize the computation time, because it's lower bound for the clock period, by relocating the flip-flops. Using retiming techniques for the synchronous data flow graphs leads high-speed digital circuits.

Retiming may either move the present registers inside design or might be accompanied by pipelining, where the designer places several registers on a cut-set line after which it applies a retiming transformation to set these registers at appropriate edges to minimize the critical path while keeping the rest of the objectives as being the secondary goal. Retiming also assists in maximizing the testability with the design [20], systematic shifting of registers across computational nodes and registers pooling of field programmable gate arrays (FPGAs) using delay transfer theorem. Tracy C. Denk et al. developed a scheduling and retiming solutions for strongly connected data-flow graph, allowing a designer look around the space of possible implementations [21].

Theorem 1: Delay transfer theorem states that, without affecting the transfer function of the system, N registers can be

transferred from each incoming edge of a node of a DFG to all outgoing edges of the same node, or vice versa.

A given dataflow graph (DFG) may be retimed using cut-set or delay transfer approaches along with the weight with the retimed path P_r could be written by-

$$\begin{aligned} P_r &= Bo \overset{eo}{\rightarrow} B1 \overset{e1}{\rightarrow} \dots\dots \overset{ek-1}{\longrightarrow} Bk \\ w_r(P_r) &= \sum_{i=0}^{k=1} w_r(e) = \sum_{i=0}^{k=1} (w(e_i) + r(B_{i+1}) - r(B_i)) \\ &= \sum_{i=0}^{k=1} w(e_i) + (\sum_{i=0}^{k=1} r(B_{i+1}) - \sum_{i=0}^{k=1} r(B_i)) \\ &= w(P_r) + r(B_k) - r(B_0) \end{aligned} \quad (2)$$

Cut-set retiming is an approach where a valid cut-set lines are placed on retime the results flow graph. A valid cutset generally is a list of forward and backward edges in a DFG intersected by the cut-set line so that if these edges are stripped from the graph, the graph becomes disjoint [2]. The cut-set retiming involves transferring quite a few delays from the edges of the identical direction across a cut-set line all edges of opposing direction over the same line without having affected the transfer function with the DFG.

Cut set retiming only affect the weights of cut from the cut set. When the two disconnected sub graphs are labeled H_1 & H_2 then cut set retiming contain adding k delay to every edge from H_1 to H_2 and removing k delay from each edge from H_2 to H_1.

Feasible solution:

$$\begin{aligned} W_r(H_1 \rightarrow H_2) &= W(H_1 \rightarrow H_2) + r(H_2) - r(H_1) \\ &= W(H_1 \rightarrow H_2) + k \end{aligned} \quad (3)$$

$$\begin{aligned} W_r(H_2 \rightarrow H_1) &= W(H_2 \rightarrow H_1) + r(H_1) - r(H_2) \\ &= W(H_2 \rightarrow H_1) - k \end{aligned} \quad (4)$$

where range of k lies between-

$$-\ min\{W(H_1 \rightarrow H_2)\} \leq\ k\ \leq\ min\{W(H_2 \rightarrow H_1)\}$$

Pipelining is a special case of case of cut set retiming where there no edge in the cut set over the sub graph H_2 to sub graph H_1 i.e. pipelining refers to graph without loops. These cut sets are mentioned as feed forward cut set. Cut-set retiming can be placed on a primary-form FIR filter to have a transposed direct-form (TDF) version using flow graph reversal theorem as shown in Fig. 2 (a).

Theorem 2: If the directions of all branches are reversed and positions of input and output are interchanged then the system function is remains unchanged.

The TDF is actually created by first reversing the direction of addition, successively placing cut-set lines on every delay edge. Each cut-set line cuts two edges from the DFG, one out of the forward and also the other in the backward direction. Then retiming moves the registers in the forward edge on the backward edge. This transforms the filter from DF to TDF. This manner breaks the critical path by placing a register before every addition operation.

In retiming, registers are systematically moved across a node derived from one edge to another. Fig. 2 (b) shows Cutset retiming structure of the FIR filter as well as DFG with a valid cut-set line. The line breaks the DFG into two disjoint graphs, one composed of nodes Q_0 and Q_1 and the other having node Q_2. The edge $Q_1 \rightarrow Q_2$ is a forward cut-set the edge, while $Q_2 \rightarrow Q_0$ and $Q_2 \rightarrow Q_1$ are backward cut-set edges.

There are two delays on $Q_2 \rightarrow Q_1$and one delay on $Q_2 \rightarrow Q_0$; one delay each is moved from these backward edges to the forward edge. The retimed DFG is minimizing the quantity of registers.

A. Min-Period and Min-Area Retiming

Min-period retiming is a clock period minimization algorithm with no consideration to the area consequence on account of an increase in the quantity of registers [15] whereas min-area retiming algorithm developed by Jia Wang et al. includes an important effect on system performance whenever a large variation within the number of registers exists [22], [23]. Mathematically in the Min - period algorithm, the minimum feasible clock period $\Phi\ (G)$ is defined to search for the retiming solution r in a way that $\Phi\ (Gr) \leq \Phi\ (G)$ for almost any retiming solution r. The feasible constraint forces the amount of delay on each edge in retimed graph to be nonnegative, as well as the critical path constraint enforces the critical path to have computation time less than or adds up to desired clock period using Flyod Warshall Algorithm.

Min-area retiming algorithm relocates the flip flops to minimize the area under given clock period while using the assumption that all registers have the same area and hence it can optimize the number of registers with additional hardware complexity. The non-negativity and period constraints in this algorithm ensure that the extra weight of each edge after retiming is nonnegative and every path whose delay is larger than the clock period has at least one register on it respectively.

Das, D. et al. presented an interlinear programming (ILP) algorithm to resolve the min-period retiming problem efficiently underneath the general delay model by formulating and solving the ILP problems incrementally [24] and located this algorithm is significantly faster and highly scalable to large circuits in term of memory consumption and running time. In improving the technique of retiming, the iteration period needs to be computed often to ascertain if a retiming is satisfied. In synchronous hard–real time systems, the device must complete execution with the current iteration before the next input sample is acquired. This imposes an upper bound on the iteration period to be less than or equal to the sampling rate of the input data. So, the complexness of computation of iteration period is a key factor compared to that of retiming algorithm.

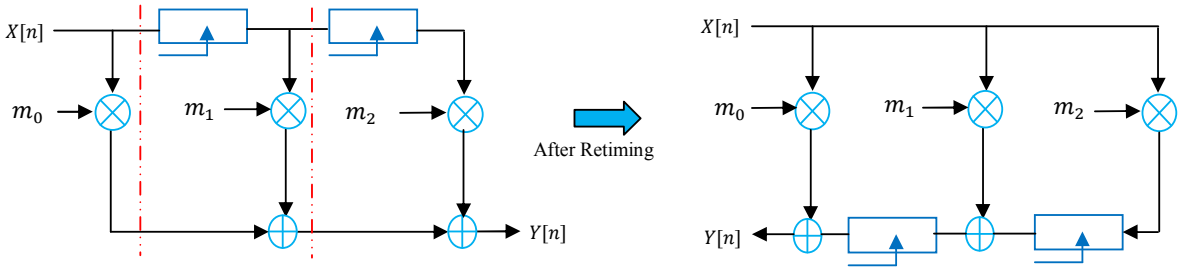

Fig. 2 (a) FIR filter and its retimed structure in Transposed direct form (TDF) for $k = 2$

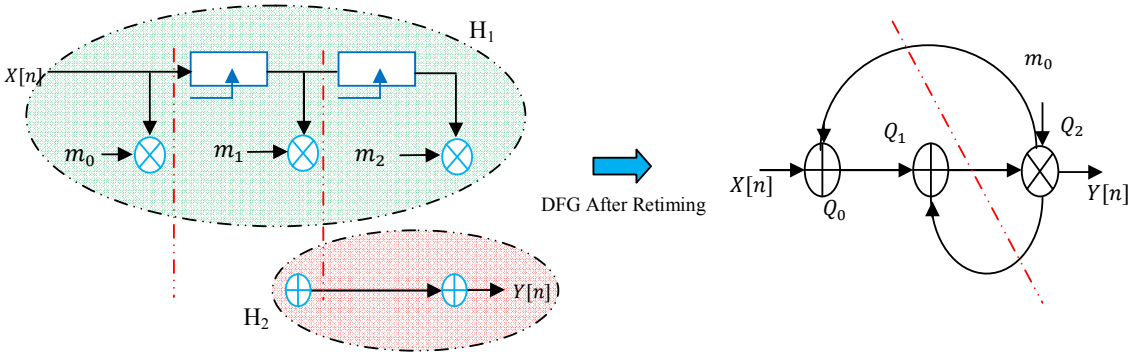

Fig. 2 (b) DFG with Cut-set Line

IV. Advance Compensation Techniques and Polyphase Implementation

Despite extremely efficient inherent multiplierless implementations of CIC filters, register overflow due to the unity feedback at every integrator stage, high power consumption on the Integrator sections on account of high sampling rate and the undesired passband droop in frequency response as a result of the need for decimation factor (N) and amount of stage (K) would be the three major problems in the practical application of comb decorators' and interpolators.

CIC compensators are single-rate or multirate lowpass filters that are accustomed to compensate the passband droop in CIC filters. The decimated version of the CIC filtered signal shows significant overlap between spectral replicas with smaller gain and larger the droop within the passband of great interest. Cascading of the CIC filter with FIR filter is among the method to compensate this droop. In this method the role on the CIC Decimator (interpolator) would be to convert the sampling rate because of the large conversion factor N, whereas the FIR filter with a magnitude response, the inverse in the CIC filter, offers the desired transition band on the overall Decimator (interpolator) and compensates the passband characteristic of the CIC filter. CIC roll-off [25] and Compensated CIC-Cosine [17] are the two advanced techniques to overcome this problem.

In CIC roll-off technique the compensation is done by rolling off the passband characteristic and minimizing the error function in the CIC filter through cascading CIC filter accompanied by a symmetric FIR filter which has a minimum order whereas in Compensated CIC-Cosine compensation technique a second order compensator filter is introduced at low rate to be able to enhance the passband of great interest on the overall filter whose coefficients are represented in canonical signed digit (CSD) form to optimize the filter structure.

The polyphase decimators used in conjunction with the multirate multistage signal processing provides efficient decimation filter structures that decimation ratio is decomposed into two factors to implement a phase error free polyphase filter structure [26]. Yonghong G. et al. [27] created a partial-polyphase architecture for CIC decimation filters using the partial-polyphase decomposition and parallel processing techniques which could operate at far lower sampling rate. IIR filters are traditionally not used in multirate decimation and interpolation applications because recursive nature. The work presents a novel methodology which enables an FIR filter use Nobel identities and effectively run for a slower clock rate in multirate decimation and interpolation applications. In polyphase implementation, the arithmetic units operate in any respect instants in the output sampling period, that is K times faster that of the input sampling period. Thus, the computational requirements on the overall structure on an Nth-order FIR filter is N multiplication and $N-1$ edition. Thus, multirate multistage techniques employed along with polyphase decimate bring about computationally efficient realizations with high power consumption cost in the Integrator stage.

V. Proposed Approach to Design CIC Decimation Filter Using Retiming Algorithm

Even as already discussed in Section II the multiplierless CIC decimation filter provides a high performance with regard

to sampling rate conversion and hardware complexity than other digital filters, however it fails to compensate the register overflow arise due feedback and desired frequency response caused by passband droop. Higher order filters provide a sharper rattle down above their pass band compared to lower order filters. Higher order filters convey more reactive elements and properly designed filter to provide much more rapid attenuation above the pass band. In this particular work we consider this to be a multirate filter design process just as one optimization problem where each requirement can contributes having a term a great error function that ought to be minimized then a high-level architectural transformation is applied at the circuit level to make up and lower the way delay of the overall system by considering a different filter order. To tackle these issues, we propose the subsequent mechanism:

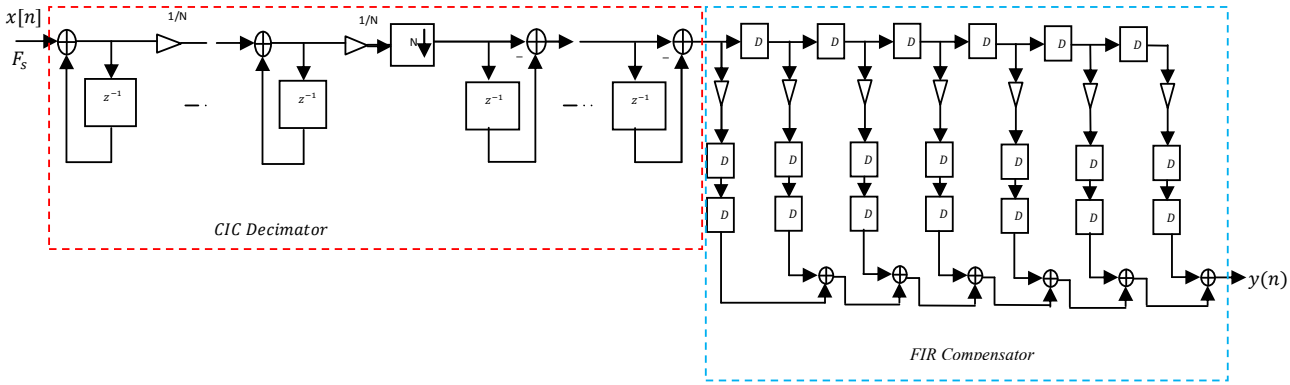

Fig. 3 Two stages Compensated CIC decimation Filter structure with retimed FIR filter of order 6

(a) First, we compensate the passband droop by cascading CIC decimation filter with FIR filter. The selection of the order and the number of stages of cascaded FIR filter needs to be optimum giving a desired frequency response inside the band of interest.
(b) Second, to generate the filter structure more effective, we introduce retiming algorithm in the compensated FIR filter.
(c) Third, we analyze the effect of filter order variation in compensated FIR filter on designed compensated CIC decimation filter structure.

VI. Performance Evaluation

A. Simulation Setup

Fig. 3 demonstrated basic setup of two stages Compensated CIC decimation Filter structure with retimed FIR filter of order 6 with the inclusion of cutset algorithm. This implemented structure enhances the filter performance in terms of its downsampling speed and computational time.

To implement this structure, we used FPGA Family: Virtex-5; Device: XC5vsx30; Package: ff324, a popular logic family regarding high packing density, low power dissipation and high yield. Each gate was assigned a maximum delay adequate to the volume of fanouts. Table I listed the various parameters utilized to setup this efficient structure. The entire operation is analyzed regarding the passband droop compensation, maximum path delay, maximum output delay and area on silicon wafers with the variation of filter order.

B. Simulation Results and Analysis

Fig. 4 and Table II demonstrated the overall magnitude response of the CIC decimation filter and retimed compensated CIC decimation filter. Initially CIC decimation filter creating a large passband droop i.e. -1.55 dB at $0.01\,\pi\frac{rad}{sample}$ without any compensation method and having even worse in high frequencies. CIC decimation filter with FIR compensation introduce an important improvement to use passband characteristic as shown in Fig. 5. Compensated CIC decimation filter with FIR compensation and polyphase FIR compensation improves the passband droop by 69.2% and 88.4% respectively at $0.001\,\pi\frac{rad}{sample}$ w.r.t. CIC decimation filter, whereas the retimed Compensated CIC Decimation Filter (length 8) improves this droop by 99.2%, 39% and 14% w.r.t. CIC decimation, compensation and polyphase filter structure respectively at $0.001\,\pi\frac{rad}{sample}$. Increase in filter length improves the desirable flat lowpass characteristic by a significant amount nevertheless the bandwidth gets reduced.

TABLE I
The Simulation Parameters

Simulation Parameters	Values
Oversampled input signal rate	1. 28 MHz
Downsampled output signal rate	20 KHz
Passband ripple (peak to peak)	0.01 dB
Sampling Frequency	48 KHz
Decimation factor	64
Input wordlength	18, 20 & 22 bits
Output wordlength	20
No. of stage of CIC decimator	1
Decimation factor of FIR decimator	8

TABLE II
PASSBAND-DROOP COMPENSATION CHART

Filter Stages with decimation Factor (D) = 64	Magnitude (dB) of Passband droop at Normalized Frequency ($\times \pi \frac{rad}{sample}$)						
	0.001	0.005	0.01	0.015	0.02	0.03	0.05
CIC decimation Filter	-0.013	-0.36	-1.55	-3.672	-6.93	-27.67	-14.38
CIC Compensation Filter	-0.004	0.004	-0.162	-1.129	-3.37	-16.35	-101.65
Compensated CIC Polyphased Decimation filter	-0.0015	-0.006	-3.012	-97.23	-101.25	-110.76	-126.73
Retimed Compensated CIC Decimation Filter, length 8	-0.0001	-0.006	-0.024	-3.153	-83.29	-100.98	-108.19

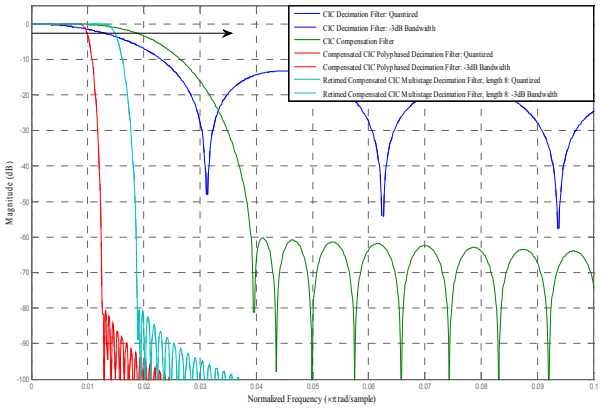

Fig. 4 Overall Magnitude Response for Decimation factor 64

This proposed filter results a trade-off between the desired compensation of the passband droop with the area and speed. The width of the passband along with the frequency characteristics beyond the passband are severely limited because the order of the filter is relatively proportional to the number of operations and therefore by selecting a low order filter, the computation time can further be reduced. Additionally, using the polyphase filter implementation, the filter can move at the lower rate in the first stage and also increasing the number of stages, the amount of passband aliasing or imaging error can be brought within the required ranges.

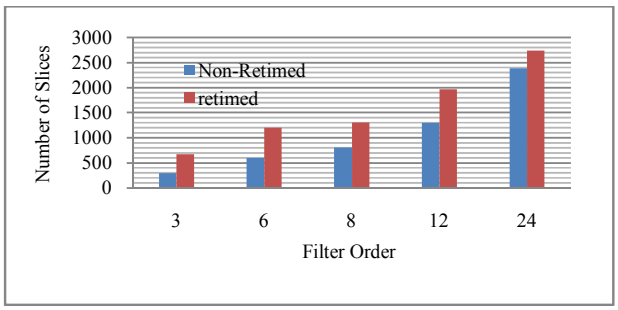

Fig. 5 (a) Comparison of Number of Slices of Non-retimed with Retimed filter

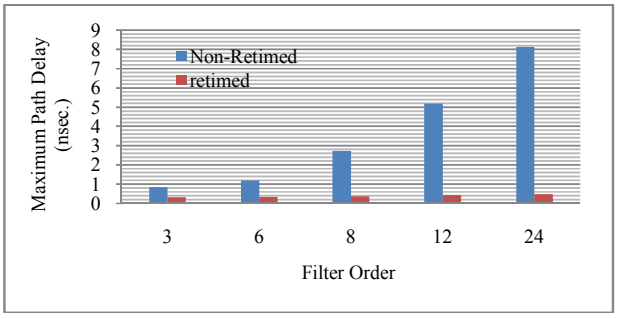

Fig. 5 (b) Comparison of Maximum Path Delay of Non-retimed with Retimed filter

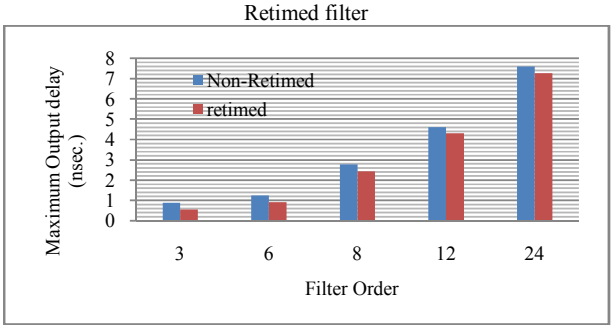

Fig. 5 (c) Comparison of Maximum Output Delay of Non-retimed with Retimed filter

Fig. 5 reveals two things: firstly, more number of slices is required in retimed structure, i.e. the chip area is increased by 55.65%, 50.45%, 38.62%, 34.19% and 13.02% for filter order 3, 6, 8, 12 and 24 respectively with retimed structure. Secondly, the Cutset retiming algorithm holds a significant improvement in path delay and total output delay by 62.27% to 94.42% and 38.04% to 4.44% respectively.

Total Number of registers, flip-flops and memory usage in retimed version is increased due to insertion of delay in filter structure and the value of logic delay becomes constant (lesser than original configuration) and independent with filter order variation.

VII. DISCUSSION AND CONCLUSION

Retiming is an important and powerful technique to optimize the performance of digital circuits. In this paper, we proposed a new approach to design a compensated CIC decimation filter using retiming algorithms to achieve efficient performance with regard to passband droop compensation and computational time. Retiming decreases the critical delays of

the circuit by changing its location to ensure that combinational path delays are balanced over the entire design. We observed that by using cutset retiming in compensator FIR filter of 3, 6, 8, 12 and 24 orders, its computation time is reduced by 38.04%, 25.78%, 12.21%, 6.69% and 4.44%, respectively compared to the non-retimed CIC compensation filter with an improvement of 39% in the passband droop. So we conclude that cut-set retiming is much suitable for high order FIR filter design as with the increase of filter order, the computation time reduces while the chip area is slightly increased. This newly designed structure provides an optimum solution for all signal processing applications which require sampling rate conversion with higher speed and flat lowpass frequency characteristic including in image and speech processing.

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