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MOSFET Based ADC for Accurate Positioning of Control Valves in Industry

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***Abstract*—**This paper presents MOSFET based analog to digital converter which is simple in design, has high resolution, and conversion rate better than dual slope ADC. It has no DAC which will limit the performance, no error in conversion, can operate for wide range of inputs and never become unstable. One of the industrial applications, where the proposed high resolution MOSFET ADC can be used is, for the positioning of control valves in a multi channel data acquisition and control system (DACS), using stepper motors as actuators of control valves. It is observed that in a DACS having ten control valves, 0.02% of positional accuracy of control valves can be achieved with the data update period of 250ms and with stepper motors of maximum pulse rate 20 Kpulses per sec. and minimum pulse width of 2.5 μsec. The reported accuracy so far by other authors is 0.2%, with update period of 255 ms and with 8 bit DAC. The accuracy in the proposed configuration is limited by the available precision stepper motor and not by the MOSFET based ADC.

***Keywords*—**MOSFET based ADC, Actuators, Positional accuracy, Stepper Motors.

I. Introduction

THERE are different types of A/D converters and each conversion method has its own set of advantages and disadvantages. Flash A/D conversion is the fastest possible way to quantize an analog signal. In order to achieve N-bits from a flash ADC, it requires 2N-1 comparators, 2N-1 reference levels. Dual slope converter gives high resolution but A/D conversion rate is low. In order to achieve N-bit resolution, a successive approximation ADC requires N clock cycles and the performance is limited by DAC linearity. The advantage of pipeline ADC is that the conversion rate does not depend on the number of stages. The disadvantage is that the circuitry is more complex. Delta–sigma converter provides very high resolution by over sampling and feedback integration but the problem is the stability. Pui-Kei Leong et al. describe the design and implementation of low power Delta-Sigma digital pulse width modulation controller for switching converters which can operate at high frequency. Smaller quantizer with a limiter is used in the digital Delta-Sigma modulator to minimize the area consumption. The resulting SNR after implementation is decreased when the input amplitude is higher than 0.9FS [1].

Jiaxin Ju et al. presented a low voltage switching capacitor DSM and focused on the implementation of unity gain and conventional DSM which could reduce the requirement of operational amplifier DC gain and was able to reduce the circuit complexity, power consumption and area. However, the SNR falls when the normalized input signal exceeds -3dB [2].

In the research paper Jonathan W. Kimball et al., a new control method for multi-phase high frequency converter is proposed. The technique combines conventional digital control, Delta-Sigma Modulation and VHF conversion techniques. The experiment results show non-linear but monotonic input-output characteristics [3].

The software control of PWM is presented in [4]-[6]. The methods require additional equipment and software. The technique proposed in this paper is simple and can give better resolution.

The proposed MOSFET ADC has high resolution, medium conversion rate suitable for the application of precise positioning of control valves in the DACS, using stepper motors as actuators. It is simple, has no DAC limiting the performance, can operate for wide range of inputs and never become unstable [4]. The error in A/D conversion is negligible, since the conversion depends on EMOSFET device characteristics.

II. MOSFET Based Analog to Digital Coding Technique

In pulse width modulation (PWM) technique, the width of the pulse at the output is proportional to the amplitude of the analog input signal, during each sampling period. Different PWM techniques are available for different applications. In this paper the ohmic region of n-channel EMOSFET is used for analog to digital coding. The locus of drain to source saturation voltage [7], $V_{DS}(sat)$ of n channel EMOSFET is related to the drain saturation current,(ID)sat by the equation;

$$(I_D)_{sat} = k_1 (V_{D(sat)})^2 \quad (1)$$

where, k_1 is a constant.

For all values of VGS VT, the drain saturation current of n channel EMOSFET is given as

$$(I_D)_{sat} = k_2 (V_{GS} - V_T)^2 \quad (2)$$

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where $k_2 = \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)$ is referred as conduction parameter. It is a function of both electrical and geometric parameters. The oxide capacitance, C_{ox} and carrier mobility, μ_n are constants for a given fabrication technology. The width to length ratio W/L, is a constant for the given geometry of MOSFET [4]. The parameter VT is the threshold voltage and VGS is the gate to source voltage.

Equating (1) and (2) we have;

$$V_{GS} - V_T = k_3 V_{DS(sat)} \quad (3)$$

where, $k_3 = k_1 / k_2$ is a constant quantity for given parameters. $k_3 = 1$ when

$$k_1 = k_2 = \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)$$

Let Vin be the analog input voltage which is to be decoded in digital form and applied gate to source voltage $V_{GS} = V_{in} + V_T$ so that the MOSFET always conduct [5]. Equation (3) can be rewritten as

$$V_{in} = k_3 \, V_{DS(sat)} \quad (4)$$

From (4) it is clear that input voltage (V_{in}) is directly proportional to $V_{DS(sat)}$, where $V_{DS(sat)}$ is a particular drain to source voltage at which drain current saturates. For a given process parameters and W/L ratio, V_{DS} (sat) varies only with V_{GS} for the MOSFET.

The MOSFET based ADC is shown in Fig. 1. V_{DD} is the power supply and is a ramp voltage. The maximum value of ramp voltage is $(V_{DS}(sat))max$ which corresponds to $(I_D)max$ of the MOSFET, and so it is safe to operate the MOSFET without any resistance connected in between V_{DD} and drain terminal. V_{in} is sampled at an interval of sampling period (update period), ts. For the i^{th} update of the input voltage, the corresponding gate to source voltage is given by

$$(V_{GS})i = (V_{in})i + V_T \quad (5)$$

During each update cycle, the ramp voltage starts from 0 V and increase with the slope of $(V_{DS(sat)})max / ts$. The ramp voltage does not cross the maximum value of $(V_{DS(sat)})max$ within the update period.

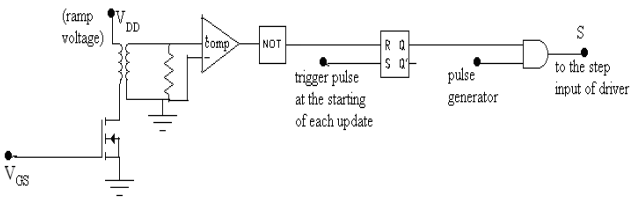

Fig. 1 Schematic diagram of MOSFET based ADC

The primary winding of the pulse transformer (having negligible resistance) is connected between the drain terminal and the ramp supply. The comparator is connected across the secondary winding. The output of the comparator is connected to the 'Reset' input of the RS flip-flop. At the starting of each data update period $(V_{GS})i$ is fed to the gate , ramp voltage is started from 0 V and RS flip-flop is set. As the ramp voltage increases the drain current also increases. This change in current produces a voltage across the primary of pulse transformer. This induces a voltage in the secondary coil and hence the comparator output will be 1. When the current is saturated (i.e. when the difference in current is zero) the induced voltage is zero and the comparator output will be 0 and the RS flip-flop is reset. When, the RS flip-flop is reset, the ramp voltage which has reached $(V_{DS(sat)}$ i, is reset to zero and will start at the starting of next update cycle. V_{ini} is proportional to $(V_{DS(sat)})i$ as per equation (4). $(V_{DS(sat)})i$ is proportional to the time duration, (tsat)i taken by the ramp voltage to reach $(V_{DS(sat)})i$. Therefore, in general for each update cycle

$$V_{in} = k_4 \, t_{sat} \quad (6)$$

where, k_4 is a parameter of dimension volt/sec. and t_{sat} is time in sec.

The RS flip-flop which is set at the starting of each update cycle is reset when the ramp voltage reaches $V_{DS(sat)}$ in the time interval of t_{sat}. Hence, the output from the RS flip-flop is pulse width modulated voltage. The width of the pulse is proportional to the input analog voltage for each update cycle. As seen from Fig. 1, the PWM output voltage is given to one input of an AND gate and a pulse generator feeds the other input. The number of pulses from the output of the AND gate, during each update cycle is proportional to V_{in}. Therefore,

$$V_{in} = k_5 N \quad (7)$$

where, k_5 is a constant and N is the number of pulses per update at the output.

III. MOSFET Based ADC Compared to Integrating ADC

In MOSFET based ADC since integration is done to generate $V_{DS(sat).}$ All the advantages of integrating type A/D converters are preserved. As in the case of integrating type ADC, the MOSFET based ADC can find wide usage because of their simplicity, ability to achieve high dynamic range, accuracy at relatively low cost, monotonic conversion with no missing codes and high frequency noise rejection due to relatively long integration of the input signal during the conversion [4], [6].

In the case of a single slope ADC, the comparison of integrator output voltage and the input analog voltage is done in a comparator which is subjected to errors like offset voltage error, gain error etc. whereas in the case of MOSFET based

ADC, the exact point at which the ramp output reaches V_{in} is identified by the saturation characteristics of n channel EMOSFET which results in less error in conversion [6]. The comparator which is used before the NOT gate is not a critical one because the input to the positive terminal of the comparator is either constant positive voltage or zero voltage. This comparator indicates only the presence or absence of signal at the input.

However, in the ramp generator of MOSFET based ADC, the error due to offset voltage in the operational amplifier and error due to dielectric absorption in the capacitor are not cancelled. In the case of dual slope ADC, the conversion rate is low since need to integrate both the input analog signal and the reference signal whereas in the case of MOSFET based ADC. There is only one integration to generate $V_{DS(sat)}$ and so the conversion rate is better. Hence the MOSFET ADC has better signal to noise ratio than single slope ADC and better conversion rate than dual slope ADC.

IV. Architecture for the Control of Actuators of Control Valves in DACS

Use either SI (MKS) or CGS as primary units. (SI units are strongly encouraged.) English units may be used as secondary units (in parentheses). This applies to papers in data storage. For example, write "15 Gb/cm^2 (100 Gb/in^2)." An exception is when English units are used as identifiers in trade, such as "3½ in disk drive." Avoid combining SI and CGS units, such as current in amperes and magnetic field in oersteds. This often leads to confusion because equations do not balance dimensionally. If you must use mixed units, clearly state the units for each quantity in an equation.

Hausila Singh et al. [8] developed a microprocessor based system in which the required form of analog or digital control signal, in the range of 4-20 mA, is generated by software means. The control signal is transmitted over a two wire system to the detector at the remote end where it is decoded and used for the control of stepper motors which are the actuators of control valves. The reported accuracy is 0.2% with 8 bit DAC and with 255ms update period.

The general form of (DACS) is shown in Fig. 2. The demand signal which specifies the extent of opening and closing of different control valves is time multiplexed using MUX in the instrumentation room. Assuming ten control valves in the DACS are need to be controlled and if 250 ms is selected as the update rate then the MUX and DEMUX will operate at the rate of 25 ms per control valve. Each control valve with its actuator has 25 ms to complete the operation during each update period. The update rate is selected in such a way that each control valve completes its operation during its multiplexing period. The standard control signal is 4-20mA. The control current which is proportional to the demand signal is passed through two wires to the remote end, denoted by terminals X and Y, where it is supposed to control the control valves. The key advantage of the current loop is that the accuracy of the signal is not affected by voltage drop in the Inter connecting wiring.

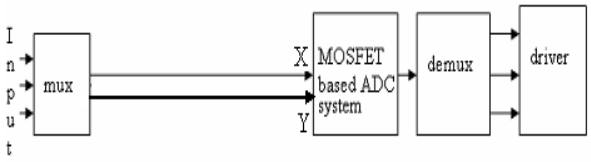

Fig. 2 Schematic diagram of multi-channel DACS

At the remote end the 4-20mA control current is fed to the proposed MOSFET based ADC system. The ADC system generates, train of pulses and direction signal during each update period (sampling period) for each control valve. The DEMUX connects the train of pulses and the direction signal to the different drivers of the actuators (stepper motors) of control valves on time shared basis. It is observed that in the DACS which need to control ten control valves, 0.02% of positional accuracy of control valves can be achieved with the data update period of 250ms and maximum stepper pulse rate of 20 Kpulses/sec and minimum pulse width of 2.5 μsec. The calculation of accuracy can be explained as follows. The range of control current is 4- 20mA, which is converted to a voltage variation of 0V-8V. The slope of the ramp voltage is selected to be 8V per 25ms. Hence, for 8V the PWM output of RS flip-flop in 25ms. The pulse period of the pulse generator is 5μsec, which is the minimum pulse period required for the stepper motor. Therefore, number of pulses which represents the range of input signal (0V-8V) is (25ms/5μs) is 5000 and hence the accuracy is 0.02%. The maximum pulse rate is 20 Kpulses/sec. which means 5000 pulses per 25ms and so maximum pulse rate specification is also satisfied.

The proposal is to develop a control unit (MOSFET based ADC system) which is simple, has high resolution, stable and conversion rate better than dual slope ADC, for DACS provided with only control valves driven by electro pneumatic drives and stepper motor drives using common 4-20mA control signal. The concept of a field bus technology [9] is too sophisticated and will be under-utilized for our application because field bus technology makes it possible to interconnect low level industrial devices, such as sensors, actuators, valves, motor starters, smart motor controllers operator interfaces and other I/O devices as well as control devices such as programmable logic controller (PLC) and computers in order to collect, and send control data/signal through a single channel.

The MOSFET based ADC system consists of (1) V0-8 control voltage generation circuit (2) MOSFET gate voltage and direction output generation circuit and (3) MOSFET based ADC circuit which is already explained in section II.

The range of control current is used to close the control valve and rotates the stepper motor in the clockwise direction. The range of current is used to open the control valve and rotates the stepper motor in the anti clockwise direction. The 4-20mA control current is passed through precision resistor to give the output 2V to 10V as the input current varies from 4 to

20mA. The output of the potentiometer is fed to the V0-8 control voltage generation circuit which is a clamper circuit. The clamper adds -2V to the input voltage and hence the output voltage variation is from 0V to 8V. Let the control valve is fully opened initially. When the V0-8 control voltage increases linearly from 0V to 4V, the control valve uniformly closes and reaches the condition of fully closed. Similarly when the V0-8 control voltage increases linearly from 4V to 8V, the control valve uniformly opens and reaches the condition of fully opened.

Let V_i and V_{i-1} represents V0-8 control voltage corresponding to the i^{th} update and $i\text{-}1^{th}$ update of the demand signal respectively. Let θ_i and θ_{i-1} are the expected angular displacements of the motor from the initial position (0 deg.) at the end of the updates. V_i and V_{i-1} are may be in closing or opening range. V_i supposed to rotate the motor from θ_{i-1} to θ_i and hence V_{GS} and direction signal to the drivers are to be generated based on the values of V_i and V_{i-1}. In the mode of continuous opening or continuous closing of valve, $V_i > V_{i-1}$. The control voltage jumps from the range to the range when the mode changes from closing to opening and vice-versa. The following conditions are needed to be satisfied by the magnitude logic circuit.

$$\text{If and then } V_{GS} = V_i - V_{\bar{i}} - 1 + V_T \quad (8)$$

$$\text{If and then VGS} = V_{GS} = V_i - V_{i-1} + V_T \quad (9)$$

$$\text{If and then } V_{GS} = V_i - V_{\bar{i}-1} - 8 + V_T \quad (10)$$

$$\text{If and then } V_{GS} = V_i - V_{\bar{i}-1} - 8 + V_T \quad (11)$$

Equations (8) to (11) in general can be written as $V_{GS} = V_{in} - V_T$, where Vin takes different values depending on the values of V_i and V_{i-1}. If the direction input is 1 to the stepper motor then the motor rotates in the clockwise direction and if the input is 0, the motor rotates in the anti-clockwise direction. The direction logic specifies the following conditions

$$\text{If } V_i \text{ then D=1} \quad (12)$$

$$\text{If } V_i \text{ then D=0} \quad (13)$$

The magnitude logic circuit satisfying conditions (8) to (11) generates V_{GS} and is fed to the gate of MOSFET decoder. The output of the MOSFET decoder is fed to the 'step input' of the stepper motor through driver. The direction logic circuit, satisfying conditions (12) and (13) generates the signal for the 'direction input' of the stepper motor.

V. Simulation Results

The MATLAB software is used for the simulation. Fig. 3 shows the different waveforms of the MOSFET based ADC. In Fig. 3 (a) is shown the sampled random analog input voltage, ranging from 0 to 1(normalized voltage), which is to be converted to digital form. Fig. 3 (b) shows the ramp voltage i.e. V_{DS}(sat) during each update period. It can be seen that the duration of the ramp voltage during each update period is directly proportional to the corresponding amplitude of the analog input signal. In Fig. 3 (c) is shown the PWM output, the pulse width of the pulse in each update period is proportional to the amplitude of the input signal. In Fig. 3 (d) is shown the number of pulses at the output. The number of pulses at the output during each update period is proportional to the analog input signal except a delay of one sampling period at the beginning. The normalized analog input voltage of 1 V is converted to 5000 digital pulses (of duration 5µsec. duration) and hence the resolution is 0.0002. The resolution will be improved by 5 times if 1µsec. pulses are used.

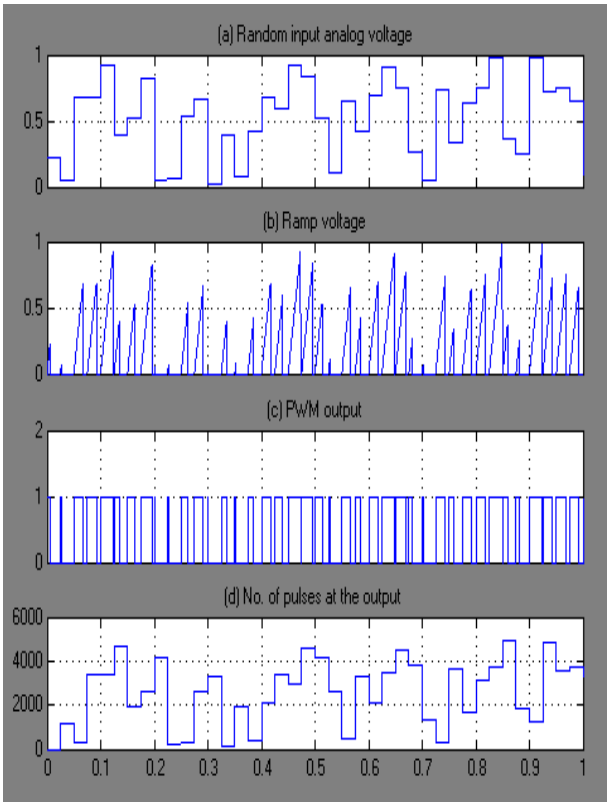

Fig. 3 Outputs of MOSFET based ADC for random control voltage. (Horizontal- Time in sec. Vertical- Voltage in volts for (a),(b), binary output for (c) and No. of pulses for (d))

VI. Conclusion

The MOSFET ADC has high resolution compared to single slope ADC and better conversion rate compared to dual slope ADC. EMOSFET characteristics are used for the conversion, which results in less error and stable operation. The MOSFET

ADC is well suited for applications in which high resolution and medium conversion rate is required with low frequency analog input signal of wide range. The MOSFET based ADC is suitable for the selected industrial application of precise positioning of control valves in industry. The positional accuracy of 0.02% for control valves can be obtained with stepper motors having pulse rate 20K pulses per second, when the update period is fixed as 250ms. The accuracy is not limited by MOSFET based ADC control technique

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