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Skin Effect: A Natural Phenomenon for Minimization of Ground Bounce in VLSI RC Interconnect

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***Abstract*—**As the frequency of operation has attained a range of GHz and signal rise time continues to increase interconnect technology is suffering due to various high frequency effects as well as ground bounce problem. In some recent studies a high frequency effect i.e. skin effect has been modeled and its drawbacks have been discussed. This paper strives to make an impression on the advantage side of modeling skin effect for interconnect line. The proposed method has considered a CMOS with RC interconnect. Delay and noise considering ground bounce problem and with skin effect are discussed. The simulation results reveal an advantage of considering skin effect for minimization of ground bounce problem during the working of the model. Noise and delay variations with temperature are also presented.

***Keywords*—**Interconnect, Skin effect, Ground Bounce, Delay, Noise.

I. Introduction

IN deep sub-micrometer technologies, the intrinsic gate delay tends to decrease dramatically. However, since the average length of global interconnect lines increases, interconnect delay dominates the overall gate delay in current deep sub-micrometer VLSI circuits [1]-[3]. As increasing operating frequency, frequency-dependence of interconnect characteristics is becoming significant. Inter-connect characteristics; especially resistance and inductance depend on frequency because of skin-effect and proximity effect. In frequency-dependent interconnects, the behavior of interconnects depends on frequency e.g. attenuation and phase velocity dispersion. In digital circuits, common input wave-form of interconnects are trapezoidal pulses. A trapezoidal pulse contains frequency components from DC to 1. More-over, the input pulse pattern is not entirely periodic. The frequency spectrum varies depending on the width of pulse and the period. The minimum pulse width and period are deter-mined by system clock. But on signal line, the pulse pattern depends on the circuit behavior. To treat frequency-dependent interconnects, several circuit models are proposed [4]-[6]. The frequency-dependent models improve simulation accuracy [5], [7], [8]. The disadvantage of the skin effect is that it attenuates the signal response, increases the resistance, and decreases the inductance. In various research impact of skin effect on delay and crosstalk noise have discussed [9]-[11]. This paper addresses the advantage side of the skin effect. For certain range of frequency when ground bounce is present in the circuit, the advantage side of skin effect can be seen if skin effect is modeled for the working of the circuit. The aim of the paper is to present the skin effect as a technique for minimizing the ground bounce present in the circuit.

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II. Skin Effect

The "Skin Effect" is the tendency of high frequency current to concentrate near the outer edge, or surface, of a conductor, instead of flowing uniformly over the entire cross sectional area of the conductor. The higher the frequency, the greater the tendency for this effect to occur is. There are three possible reasons we might care about skin effect:-

1. The resistance of a conductor is inversely proportional to the cross sectional area of the conductor. If the cross sectional area decreases, the resistance goes up. The skin effect causes the effective cross sectional area to decrease. Therefore, the skin effect causes the effective resistance of the conductor to increase.
2. The skin effect is a function of frequency. Therefore, the skin effect causes the resistance of a conductor to become a function of frequency (instead of being constant for all frequencies.) This, in turn, impacts the impedance of the conductor.
3. If the skin effect causes the effective cross sectional area of a trace to decrease and its resistance to increase [12].

Fig. 1 clearly defines how at high frequencies the skin effect can be visualized in a simple conducting wire. Fig. 1 is self capable of explaining how the resistance due to skin effect increases in the presence of skin effect [13].

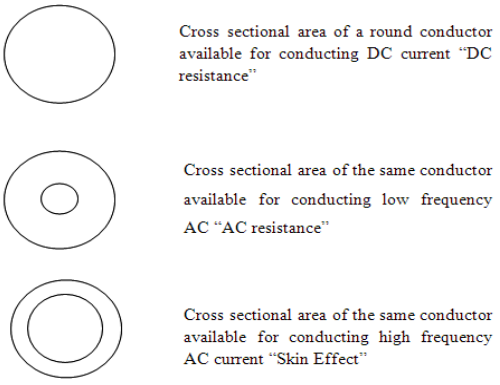

Fig. 1 Cases of Uniform Current Density and Current Density Impacted By "Skin Effect"

In the first case of the figure it is clearly shown that when no skin effect is encountered in the wire the current density is

quite uniform within the cross sectional area. But as soon as the frequency is increased the effective cross sectional area for the current density and current conduction decreases and at very high frequency the current starts to flow from the skin of the conductor. This effect is known as "Skin Effect".

III. Ground Bounce

In some recent years the Ground Bounce has been a great concern of researchers. As the integration of the devices on a chip has reached to the nm regime and frequency of operation of the devices has achieved a range of GHz, the study to consider and model the ground bounce has become important to consider [14]. The cause of ground bounce can be understood from Fig. 2.

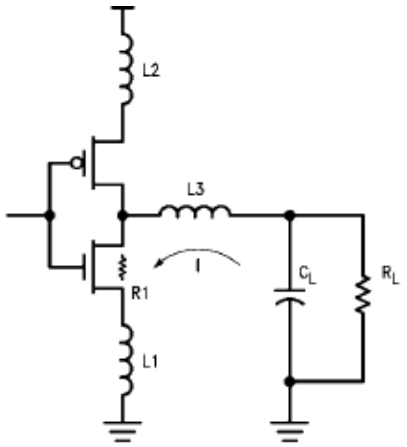

Fig. 2 Circuit Victim of Ground Bounce [14]

In order make the voltage transition from High to Low and Low to High it is required that the current flowing in the circuit charges and discharges the capacitor. The inductor present in the circuit experience a voltage induced. This voltage can be expressed as below:

$$V_L(induced) = L \cdot \left(\frac{dI}{dt}\right) \quad (1)$$

where, I is the current flowing in the circuit. L is the inductor across which the induced voltage is to be measured. This induced voltage affects the internal threshold voltage to change. The internal ground level for inductor due to this induced voltage gets shifted. This is known as "Ground Bounce" [14].

There are two major inductive components which contribute to the total ground bounce: the inductive noise due to the on-chip interconnects, and the inductive noise due to the chip package interface consisting of bond wire self-inductance, trace and pin self-inductances, and trace-to-trace mutual inductance [15]. More recently a number of researchers have tried to consider the short channel effects of MOS devices on the ground bounce waveform [16]-[18].

IV. Proposed Model for Measuring and Minimizing Ground Bounce

The proposed model for measuring and analyzing ground bounce is shown in Fig. 3. The proposed model is using RC global interconnect. As it is described in Section II, the ground bounce occurs whenever there is a transition from a high to low or a low to high due to the voltage induced in the inductor.

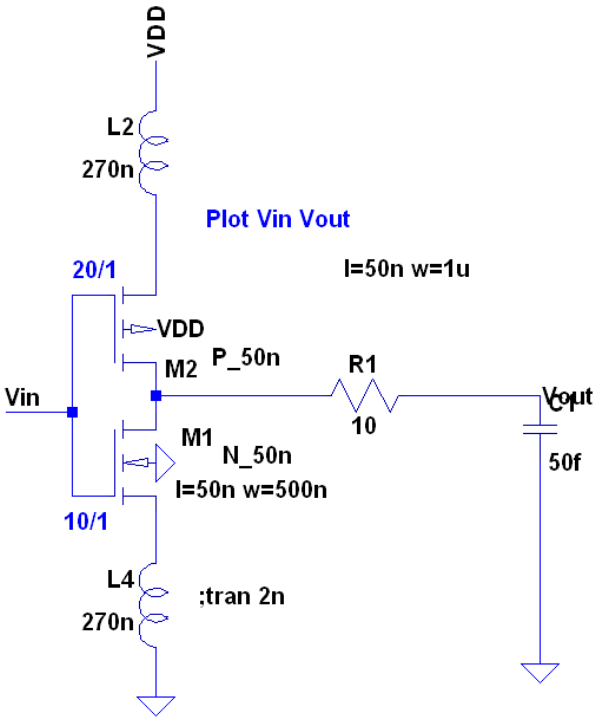

Fig. 3 Proposed Model of a CMOS inverter with RC Interconnect for Measuring and Minimizing Ground Bounce

The proposed model is used to analyze the Ground Bounce with a RC interconnect segment without skin effect and then the same model is used to highlight the output with minimized ground bounce in the presence of "Skin Effect". Since when the circuit is operating at higher frequency in GHz in the presence of Skin Effect, the resistance becomes a frequency dependent element. The resistance in the presence of Skin Effect is given by following equations [13].

$$R_{total} = R_{DC} + \sqrt{f}\, R_{AC} \quad (2)$$

$$R_{DC} = \frac{\rho L}{W.t} \quad (3)$$

$$R_{AC} = \frac{\rho L}{A_{current\ density\ area}} = \frac{L\rho}{\omega\sqrt{\frac{2}{\omega\sigma\mu}}} = \frac{L\sqrt{\rho}}{\omega\sqrt{2}}\sqrt{\mu f} \quad (4)$$

$$R = R_{total} = \frac{\rho L}{Wt} + \frac{L\sqrt{\rho}}{\omega\sqrt{2}} \cdot \sqrt{\mu f} \quad (5)$$

where,

W Width of the conductor
T Thickness of the
L Length of the conductor
μ Permeability of conductor
σ Conductivity of conductor
ρ Resistivity of conductor
ω Frequency of current

V. Simulation Results

This section describes the results obtained when the proposed model is simulated in the presence and in the absence of Skin Effect. Section IV has described that at higher frequency the resistance becomes frequency dependent. The same concept is applied here to reduce the ground bounce. The level of Ground Bounce in the absence of Skin Effect is described by Table I, whereas the level of Ground Bounce in the presence of Skin Effect is described by Table II.

TABLE I
Ground Bounce Level and Delay in the Absence of Skin Effect

V_{in}	R(K)	V_{GBP}(V)		t (ns)	
		0->1	1->0	1->0	0->1
1	1	1.131	0.044	1.411	2.042
1.5	5	0.941	0.041	1.442	2.337

TABLE II
Ground Bounce Level and Delay in the Presence of Skin Effect

V_{in}	R(K)	V_{GBP}(V)		t (ns)	
		0->1	1->0	1->0	0->1
1	1	1.131	0.044	1.411	2.042
1.5	5	0.941	0.041	1.442	2.337

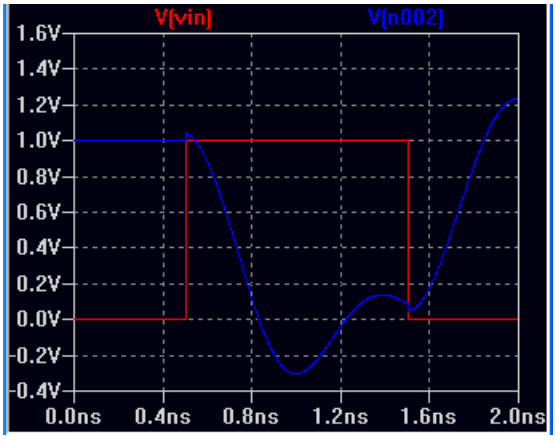

Fig. 4 Ground Bounce voltage level in the absence of skin effect

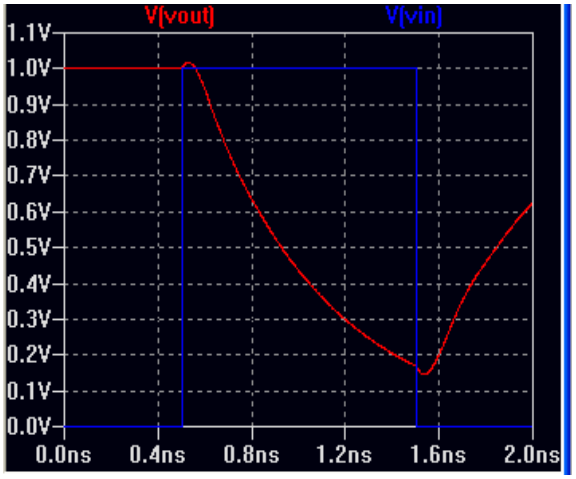

Fig. 5 Ground Bounce voltage level in the presence of skin effect

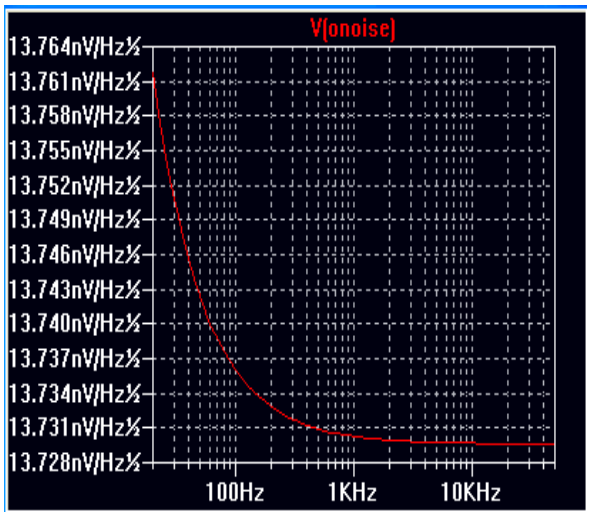

Fig. 6 Output Noise in the presence of skin effect

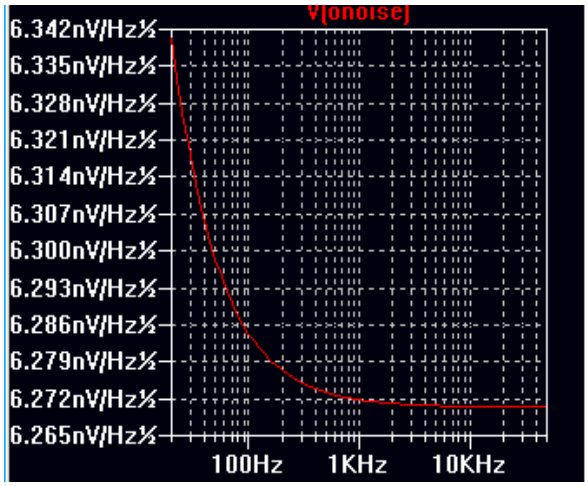

Fig. 7 Output Noise in the absence of skin effect

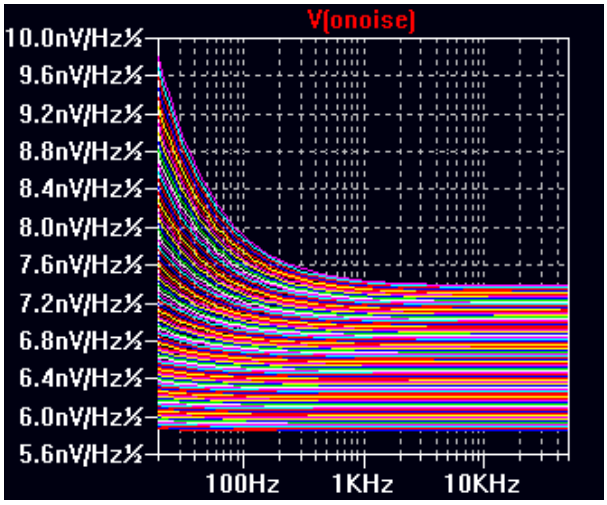

Fig. 8 Output Noise with temperature rising form (0-1000C) in the absence of skin effect

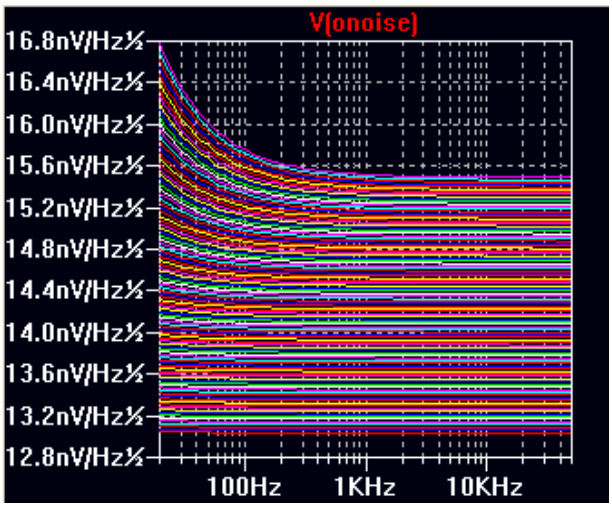

Fig. 9 Output Noise with temperature rising form (0-1000C) in the presence of skin effect

The motive of this paper is to highlight one of the advantages of an undesired effect that occurs at higher frequency. Skin effect has been proved as an effect which makes an adverse effect on delay, crosstalk noise and bandwidth but its advantage has never been tried to find out in previous research. Skin Effect has an adverse effect on resistance, so resistance increases with frequency. The same concept can be used to model skin effect when ground bounce is of great concern. If the skin effect is carefully considered during the working of circuit where ground bounce is occurring at output in that situation the skin effect will nullify the peaks of ground bounce up to a great extent.

Fig. 4 has explained the presence of ground bounce when skin effect has not been considered. The simulation graph explains that there are peaks of ground bounce at the output. The simulation graph shown in Fig. 5 explains the minimized ground bounce at the output when skin effect is considered. But still there is a trade of between the minimization of ground bounces and output noise. The simulation graph shown in Fig. 6 explains that when the skin effect is considered the noise present at output noise has a highest peak at the very initial condition when the circuit starts to work. In opposite to the above description the circuit output noise in the absence of skin effect has a low level of noise Fig. 7. Graphs shown in Figs. 8 and 9 show the variation of output noise when the temperature has a range of variation from 0-100^{0}C.

Table I is self explanatory that when the skin effect is not considered during the transition of 1 to 0 and 0 to 1 the level of ground bounce peak voltage is higher whereas the level of ground bounce peak is reduced in Table II when skin effect is considered. Despite the reduction of voltage peak a little increment in delay is observed.

VI. Conclusion

This article strives to highlight that modeling of skin effect can be an advantage when there is a drastic change in the circuit characteristics due to the Ground Bounce. Modeling of one of the undesired effect at which occurs at higher frequency can be a solution to this problem of ground bounce. Modeling of skin effect reduces the need to add more transistors in certain topology to reduce the ground bounce instead a careful modeling and proper consideration to skin effect can work to minimize the ground bounce. Moreover efforts are required to reduce delay and noise. Consideration of skin effect to minimize the ground bounce will reduce the area requirement raised by the involving more transistors for reducing the ground bounce. Simulation results demonstrate the validity of the concept.

References

[1] D. A. Priore, “Inductance on Silicon for Sub-Micron CMOS VLSI,” in Proc. IEEE Symp. On VLSI Circuits, pp. 17-18, May (1993).
[2] M. P. May, A. Taflove, and J. Baron, “FD-TD Modeling of Digital Signal Propagation in 3-D circuits with Passive and Active Loads”, IEEE Trans. Microwave Theory Tech., Vol. 42, pp. 1514-1523, Aug. (1994).
[3] S. Mei, C. Amin and Y. I. Ismail, “Efficient Model Order Reduction Including Skin Effect”, Proc. IEEE, pp. 232-237, June (2003).
[4] H. A. Wheeler, “Formulas for the Skin-Effect,” Proc. of Institute of Radio Engineers, Vol.30, pp.412–424, Sept (1942).
[5] B. Krauter and S. Mehrotra, “Layout Based Frequency Dependent Inductance and Resistance Extraction for On-Chip Inter-connect Timing Analysis”, Proc. DAC, pp.303–308, (1998)
[6] D. B. Kuznetsov and J. E. Schutt-Aine, “Optimal Transient Simulation of Transmission Lines”, IEEE Trans. CAS, Vol.43, Issue.2, pp.110–121, Feb (1996).
[7] A. Deutsch, P. W. Coteus, G. V. Kopcsay, H. H. Smith, C. W. Surovic, B. L. Krauter, D. C. Edelstein, and Phillip J. Restle, “On-Chip Wiring Design Challenges for Gigahertz Operation,” Proc. of IEEE, Vol.89, Issue.4, pp.529–555, Apr (2001).
[8] A. Tsuchiya, M.Hashimoto and H.Onodera, “Representative Frequency for Interconnect R(f)L(f)C Extraction”, Proc. of IEEE, pp. 691-696, Jan (2004).
[9] V. Maheshwari, S. Lavania, R. Kar, D. Mandal and A. K. Bhattacharjee, “Modelling of Skin Effect in On-Chip VLSI RLC Global Interconnect”, Journal of VLSI Design Tools & Technology,Volume 1, Issue 1, (2011).
[10] V. Maheshwari, S. Lavania, D. Sengupta, R. Kar, D. Mandal, A. K. Bhattacharjee, “An Explicit Crosstalk Aware Delay Modelling For On-Chip VLSI RLC Interconnect With Skin Effect” Journal of Electronic Devices, Frans, Vol.10, pp.499-505,(2011).

[11] S. Lavania and V. Maheshwari, "An Explicit Crosstalk Aware Delay Modelling for On-Chip RLC Interconnect for Ramp Input with Skin Effect" International Journal Of Engineering and Research Applications,Vol.1, Issue 4, pp.1352-1359, (2011).
[12] Skin Effect Douglas Brooks, Ultracad Design, Inc. Avaliable at http://www.ultracad.com, (online 2012).
[13] S. Lavania and S. K. Sharma, "Skin Effect in High Speed VLSI On-chip Interconnects", International Conference on VLSI, Communication & Networks, Proc. V-CAN, (2011).
[14] Technical Report on "Understanding & Minimizing Ground Bounce", Document No. AN-640, Fairchild Semiconductor, Available at www.fairchildsemi.com/an/AN/AN-640, Revised on Feb (2003).
[15] P. Heydari and M. Pedram, "Ground Bounce in Digital VLSI Circuits", IEEE Trans. On VLSI Systems, Vol.11, Issue.2, pp.180 – 193, (2003).
[16] S. R. Vemuru, "Accurate Simultaneous Switching Noise Estimation Including Velocity-Saturation Effects", IEEE Trans. On Comp., Package and Manufacturing. Technol. - Part B, Vol.19, Issue.2, May (1996).
[17] S. Jou, W. Cheng and Y. Lin, "Simultaneous Switching Noise Analysis and Low Bouncing Design", IEEE Custom Integrated Circuit Conference, pp. 25.5.1-25.5.4, May (1998).
[18] H. Cha and O Kwon, "A New Analytic Model of Simultaneous Switching Noise in CMOS Systems", IEEE Proc. Electronic. Comp. and Technology Conference, pp. 615-621, May (1998).

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