

Two Active Elements Based All-Pass Section Suited for Current-Mode Cascading

J. Mohan and S. Maheshwari

Abstract—A new circuit topology realizing a first-order current-mode all-pass filter is proposed using two dual-output second generation current conveyor and two passive components. The circuit possesses low-input and high-output impedance, which makes it ideal for current-mode systems. The proposed circuit is verified through PSPICE simulation results.

Keywords—active filter, all-pass filter, current-mode, current conveyor.

I. INTRODUCTION

THE circuits with current input, current output are termed as current-mode circuits. Such circuits demand a basic requirement to be of practical use in any larger current-mode system. This requirement is in terms of the input and output impedances which are desirably low and high respectively. Besides, input impedance should be low in comparison to the output impedance in order to avoid loading problems when cascading such circuits to form larger systems. All-pass filters are an important class of analogue signal processing functions with applications in communication and instrumentation systems [1] - [2]. Numerous current-mode all-pass sections (CM-APSs) employing different types of active elements, such as current conveyors and its different variations have been reported in the literature [3]- [22]. Despite a number of first order CM-APSs, there is a need to further explore new topology, keeping the following points into consideration

- Use of optimum passive elements.
- Use of grounded capacitor.
- Low-input and high-output impedance
- Simple configuration

The technical literature shows that none of the recently reported works provide all the above features simultaneously. Most of the circuits uses single active element and offer high output impedance feature together but employ more than two passive components [3], [6], [12], [16]. Though the circuits described in [5], [9], [14], [18], [19] fall in the separate category of tunable, resistorless realizations, the most recent of these [18], [19] enjoys low input and high output impedance. On the other hand, some of the circuits employ single active element and two passive components [8], [11], [15], [17]. Such circuits aim at realizing the first order all-pass function using optimum number of active and passive components, rather than offering low input and high output impedance. The

vast majority of the circuits offer high output impedance [3], [6], [7], [10], [12], [13], [15]- [17]. Some of the circuits employ floating capacitor [3], [7], [10] - [12], [16], which is not desirable for IC implementation [23]. Though the recently presented circuits in [20], [21] uses three grounded passive components with matching conditions but enjoys low-input and high-output impedances.

This paper presents a new circuit topology which realizes a first-order current-mode all-pass section, with low-input and high-output impedance and employs a grounded capacitor and a resistor. The proposed circuit is based on dual-output plus-type second generation current conveyor (DO-CCII+), which is modified from second generation current conveyor (CCII) [24]. CCII is a device which can operate both in voltage and current-modes, providing flexibility to a variety of analog signal processing circuits. In addition it can offer advantageous feature such as wider signal bandwidth, higher slew-rate, greater linearity and low power consumption. The implementation configuration of the DO-CCII+ is simpler than that of a CCII± (plus and minus type together). Infact, the number of transistors in DO-CCII+ is decreased by four with respect to the CCII± [22]. The cascable circuit presented in [22] employs two CCII±, one grounded capacitor and one grounded resistor with a feature of high-input and low-output impedances. PSPICE simulation results using $0.5\mu m$ CMOS parameters are given to validate the circuits.

II. PROPOSED CIRCUIT

A DO-CCII+ with two Z+ outputs is characterized by the following relationship

$$V_X = V_Y, I_{Z1+} = I_{Z2+} = I_X, I_Y = 0 \quad (1)$$

where the suffixes refer to the respective terminals. The DO-CCII+ is characterized by high input impedance at the Y terminal, high output impedance at the Z1+ and Z2+ terminals and low impedance at the X terminal. The symbol and CMOS implementation of the DO-CCII+ are shown in Fig. 1 and 2 [24].

The new proposed circuit using two DO-CCII+ and two passive components is shown in Fig. 3. The circuit is characterized by the following current transfer function

$$\frac{I_{OUT}}{I_{IN}} = -\left(\frac{s - (\frac{1}{CR})}{s + (\frac{1}{CR})}\right) \quad (2)$$

Equation (2) is the standard current transfer function for a first order all-pass filter with unity gain and frequency dependent phase function (ϕ) with a value $\phi = -2\tan^{-1}(RC)$ and

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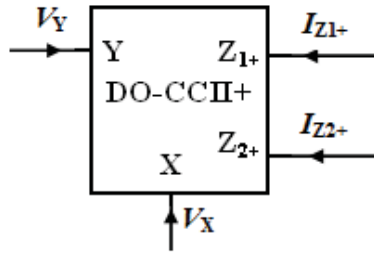


Fig. 1. Symbol of DO-CCII+

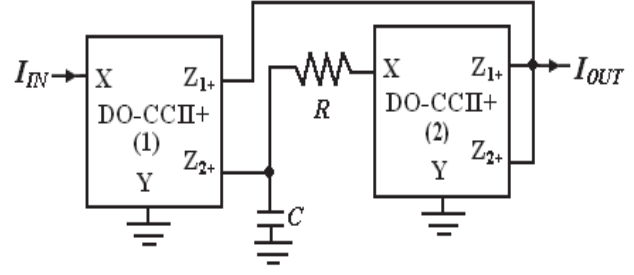


Fig. 3. 2 Proposed current mode cascadable all pass -filter

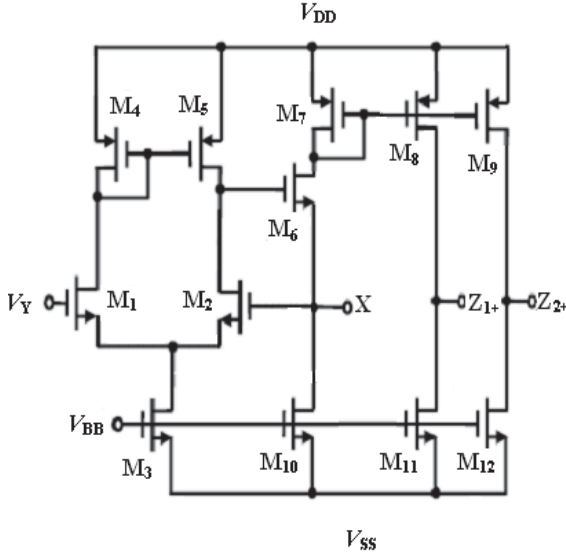


Fig. 2. CMOS Implementation of DO-CCII+

angular pole frequency, $\omega_o = 1/RC$. The salient features of the proposed circuit are low-input and high-output impedance, and optimum use of passive components i.e a resistor and a grounded capacitor. These two features are not exhibited together in any of the cited works [2], [3], [5]-[7], [8]-[13], [15]-[17], [20], [21].

III. NON-IDEAL ANALYSIS

The non-ideal DO-CCII+ is characterized by the following relationships:

$$V_X = \alpha_k V_Y, I_{Z1+} = +\beta_{k1} I_X, I_{Z2+} = +\beta_{k2} I_X, I_Y = 0 \quad (3)$$

where, $\alpha_k(s)$ represent the frequency transfer of the internal voltage follower and $\beta_{k1}(s)$, $\beta_{k2}(s)$ represent the frequency transfers of the internal current followers of the k th-DO-CCII+, respectively. They can be approximated by first-order low pass functions, which can be considered to have a unity value for frequencies[25]. If this circuit is working at frequencies much less than the corner frequencies of $\alpha_k(s)$, $\beta_{k1}(s)$ and $\beta_{k2}(s)$ namely, then $\alpha_k(s) = 1 - \varepsilon_{kv1}$ and $\varepsilon_{kv1} (|\varepsilon_{kv1}| \ll 1)$ denotes the voltage tracking error from the Y terminal to the X terminal of the k thDO-CCII+; $\beta_{k1}(s) = \beta_{k1} = 1 - \varepsilon_{ki1}$ and $\varepsilon_{ki1} (|\varepsilon_{ki1}| \ll 1)$ denotes the current tracking

error from the X terminal to the Z1+ terminal; $\beta_{k2}(s) = \beta_{k2} = 1 - \varepsilon_{ki2}$ and $\varepsilon_{ki2} (|\varepsilon_{ki2}| \ll 1)$ denotes the current tracking error from the X terminal to the Z2+ terminal of the k thDO-CCII+. Analysis of the circuit using this description yields the following current transfer function:

$$\frac{I_{OUT}}{I_{IN}} = -\beta_{11} \left(\frac{s - \left[\frac{\beta_{12}(\beta_{21} + \beta_{22} - \beta_{11})}{\beta_{11}} \right] \left(\frac{1}{CR} \right)}{s + \frac{1}{CR}} \right) \quad (4)$$

It is easily verified that for the ideal case these gains are unity and (4) reduces to the ideal (2). However, the non-idealities do affect the filter gain, as it now depends on β_{11} but the pole frequency is unaltered by DO-CCII+ non-idealities. The active and passive sensitivities of the proposed CM-APS are derived from (4), which are as follows:

$$\begin{aligned} S_{C,R}^{\omega_0} &= -1 \\ S_{\alpha_1, \alpha_2, \beta_{11}, \beta_{12}, \beta_{21}, \beta_{22}}^{\omega_0} &= 0 \\ S_{\alpha_1, \alpha_2, \beta_{12}, \beta_{21}, \beta_{22}}^H &= 0 \\ S_{C,R}^H &= 0 \\ S_{\beta_{11}}^H &= 1 \end{aligned} \quad (5)$$

From the results it is evident that the sensitivities are within unity in magnitude, thus ensuring a good sensitivity performance.

IV. EFFECT OF PARASITICS

The practical current conveyors have various parasitics at their Y, Z and X terminals. The main amongst these are the Y and Z terminals parasitic capacitances and the X terminal resistance [25]. The proposed circuit is reanalyzed by considering the above parasitic effects; the following transfer function is obtained

$$\frac{I_{OUT}}{I_{IN}} = - \left(\frac{s - \left(\frac{1}{(C + C_{Z21+})(R + R_{X2})} \right)}{s + \left(\frac{1}{(C + C_{Z21+})(R + R_{X2})} \right)} \right) \quad (6)$$

where C_{Z21+} is the parasitic capacitance at the Z2+ terminal of DOCCII+(1) and R_{x2} is the parasitic resistance at the X-terminal of DOCCII+(2).

From (6), it is seen that the parasitic capacitance at Z2+ terminal of conveyor (1) merges with external capacitor (C) and the parasitic resistance at X terminal of conveyor (2) merges with external resistor (R). So, the proposed circuit enjoys a structure where the effects of various parasitics are absorbed by the external components. A slight deviation in pole frequency from the designed values can be expected because of the parasitics.

V. SIMULATION RESULTS

PSPICE simulations were performed using the CMOS realization of DO-CCII+ (Fig. 2) with MOSIS 0.5 μm CMOS parameters and aspect ratios as given in Table I and Table II. The supply voltages used were $\pm 2.3\text{V}$ and $V_{BB} = -1.8\text{V}$. The circuit of Fig. 3 was designed with $R = 5\text{K}\Omega$, and $C = 1\text{pF}$. The gain and phase responses are shown in Fig. 4, where a pole frequency of 30.349 MHz is obtained. This is close to the theoretical value of 31.84 MHz. The circuit was next used as a phase shifter introducing a 90° phase shift to a sinusoidal voltage signal of $10\text{ }\mu\text{A}$ peak at 31.84 MHz. The input and 90° phase-shifted output waveforms are given in Fig. 5 and in the Lissajous pattern of Fig. 6, which verifies the circuit as a phase-shifter. The Fourier spectrum of input signal and output signal are shown in Fig. 7. The total harmonic distortion (THD) variation at the output by varying the amplitude of the input current at a frequency 31.84 MHz is shown in Fig. 8.

TABLE I
0.5 μm CMOS PARAMETERS

NMOS:	LEVEL=3 UO=460.5 TOX=1.0E-8 TPG=1 VTO=0.62 JS=1.8E-6 XJ=0.15E-6 RS=417 RSH=2.73 LD=0.04E-6 ETA=0 VMAX=130E3 NSUB=1.71E17 PB=0.761 PHI=0.905 THETA=0.129 GAMMA=0.69 KAPPA=0.1 AF=1 WD=0.11E-6 CJ=76.4E-5 MJ=0.357 CJSW=5.68E-10 MJSW=0.302 CGSO=1.38E-10 CDDO=1.38E-10 CGBO=3.45E-10 KF=3.07E-28 DELTA=0.42 NFS=1.2E11
PMOS:	LEVEL=3 UO= 100 TOX = 1.0E-8 TPG = 1 VTO = -0.58 JS = 38E-6 XJ = 0.1E-6 RS = 866 RSH = 1.81 LD = 0.03E-6 ETA = 0 VMAX = 113E3 NSUB = 2.08E17 PB = 0.991 PHI = 0.905 THETA = 0.120 GAMMA = 0.76 KAPPA = 2 AF=1 WD= 0.14E-6 CJ = 85E-5 MJ = 0.429 CJSW = 4.67E-10 MJSW = 0.631 CGSO = 1.38E- 10 CGDO = 1.38E-10 CGBO = 3.45E- 10 KF = 1.08E-29 DELTA = 0.81 NFS = 0.52E11

TABLE II

ASPECT RATIOS USED IN FIG. 3

MOS Transistors	$W(\mu\text{m})$	$L(\mu\text{m})$
M_1, M_2	20	1
M_3	50	2.5
M_4, M_5	60	2.5
M_6	40	0.5
M_7, M_8, M_9	20	2.5
M_{10}, M_{11}, M_{12}	20	2.5

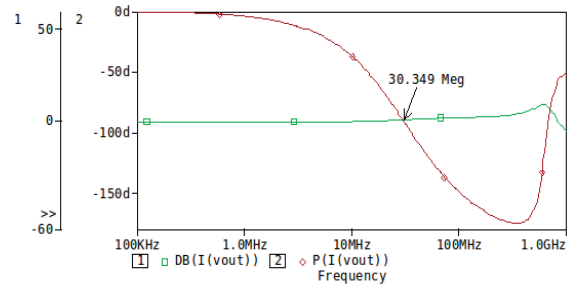


Fig. 4. Simulated Gain and Phase Response for Fig.3

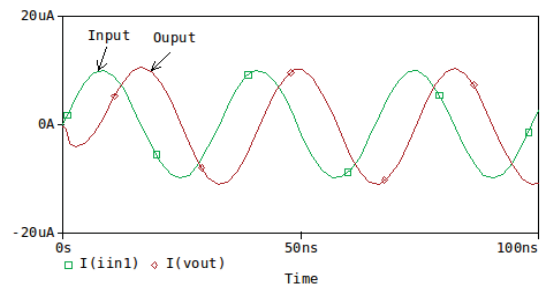


Fig. 5. Input and 90° phase shifted output at 31.84 MHz

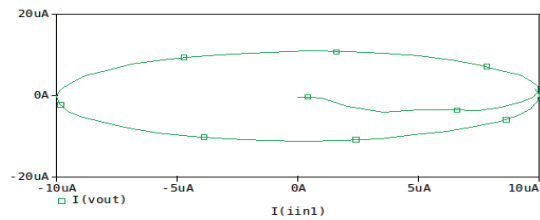


Fig. 6. Lissajous Pattern (I_{out} against I_{IN}) for Fig.3

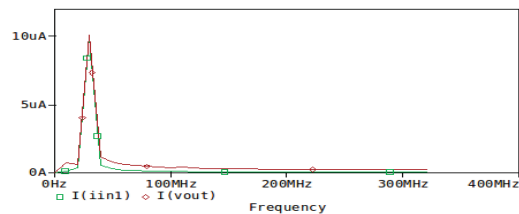


Fig. 7. Fourier spectrum of the input and output signal

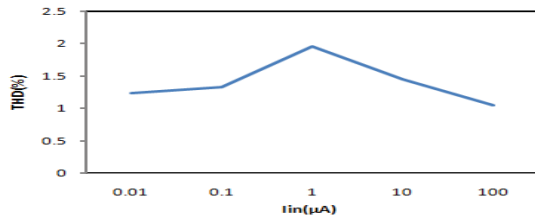


Fig. 8. THD variation with input signal at 31.84 MHz

VI. CONCLUSION

This paper presented a new first-order current-mode all-pass filter, employing two DO-CCII+s and two passive components. The circuit enjoys low-input and high-output impedance feature, which is desirable for Current-mode circuits. The circuit uses optimum passive components i.e a resistor and a grounded capacitor. The proposed circuit with grounded capacitor is suited for IC implementation in CMOS technology and is verified through PSPICE simulations using MOSIS 0.5 μm CMOS parameters. The new reported circuit further add to the repertoire of CCII based works [21],[22].

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