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CMOS-Compatible Plasmonic Nanocircuits for On-Chip Integration

Shiyang Zhu, G. Q. Lo, and D. L. Kwong

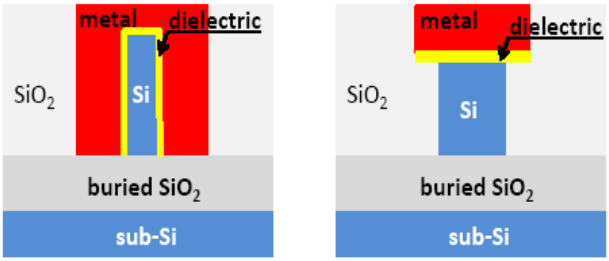
***Abstract*—**Silicon photonics is merging as a unified platform for driving photonic based telecommunications and for local photonic based interconnect but it suffers from large footprint as compared with the nanoelectronics. Plasmonics is an attractive alternative for nanophotonics. In this work, two CMOS compatible plasmonic waveguide platforms are compared. One is the horizontal metal-insulator-Si-insulator-metal nanoplasmonic waveguide and the other is metal-insulator-Si hybrid plasmonic waveguide. Various passive and active photonic devices have been experimentally demonstrated based on these two plasmonic waveguide platforms.

***Keywords*—**Plasmonics, on-chip integration, Silicon photonics.

I. Introduction

SILICON photonics, where photonics devices are fabricated using Si CMOS compatible materials and the manufacturing is based on the available microelectronics infrastructure, is merging as a unified platform for driving photonic based telecommunications and for local photonic based interconnect [1]. One critical issue for the seamless integration of electronics and photonics in a single chip is the significantly larger size of the photonic devices as compared with the electronic devices due to the fundamental diffraction limit as well as the relatively weak optical response in Si. A potential solution for this issue is to exploit the special physics of surface plasmon polariton (SPP) propagating in metal dielectric structures (namely, plasmonics) because the SPP waveguides can confine the optical mode far beyond the diffraction limit, thus enabling to reduce the dimension of optical devices to comparable to electronic devices [2]. Moreover, the incorporation of metal and dielectrics in plasmonics may provide additional potential to design novel photonic devices. However, the SPP waveguides suffer from a fundamental tradeoff between the tight mode confinement and the long propagation loss due to the inevitable metal loss. To overcome this tradeoff, on one hand, one needs to improve the propagation distance of plasmonic waveguide without sacrificing the confinement by optimization of waveguide structure and material property, and on the other hand, one needs to implement both plasmonics and conventional dielectric waveguide based photonics in the same chip so that the plasmonic waveguides will be used to realize functional ultracompact plasmonic devices while the conventional dielectric waveguide will be used to propagate the optical signal over a long distance.

Various plasmonic waveguide structures as well as passive and active plasmonic devices based on these plasmonic waveguides have been proposed and/or demonstrated with their own advantages and disadvantages [3]. In this paper, we present two CMOS-compatible plasmonic waveguide platforms as shown schematically in Fig. 1. One is the horizontal metal-insulator-Si-insulator-metal (MISIM) nanoplasmonic waveguide [4], [5] and the other is the vertical metal-insulator-Si (MIS) hybrid plasmonic waveguide [6]. Both plasmonic waveguides are inherently a typical MOS capacitor, thus enabling to actively modulate the propagation property by an external voltage applied between the metal cover and the Si core.



(a) (b)

Fig. 1 Two CMOS compatible plasmonic waveguide platforms for plasmonic nanocircuits: (a) horizontal metal-insulator-Si-insulator-metal (MISIM) nanoplasmonic waveguide, and (b) vertical metal-insulator-Si (MIS) hybrid plasmonic waveguide.

II. Experimental

The metal used in plasmonics is usually Ag or Au because they provide a relatively low metal loss at 1.55μm telecom wavelengths. However, both Ag and Au are not CMOS compatible. Among the CMOS-compatible metals, it has found that Cu is the best choice for 1.55μm telecom wavelengths due to its relatively low metal loss around this wavelength [7]. Therefore, Cu is used as the metal in this work. The plasmonic devices based on the above two plasmonic waveguides can be fabricated with a similar fabrication flow, as shown schematically in Fig. 2 except that some additional steps (i.e., SiO_2 deposition and chemical mechanical polishing) are required for the MIS waveguides.

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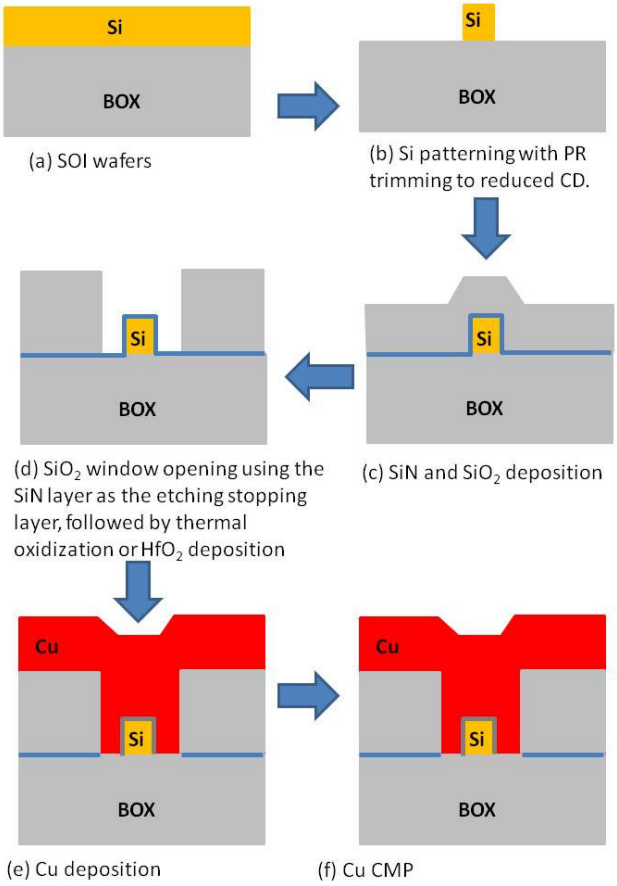

Fig. 2 Schematic fabrication flow for the MISIM plasmonic waveguide, the MIS plasmonic waveguide can be fabricated using similar flow but with additional SiO_2 deposition and CMP steps

Both plasmonic waveguides are inserted in conventional Si channel waveguides with a tapered coupler, as shown schematically in Fig. 3 (a). Fig. 3 (b) shows photography of a final chip. The Cu covered area is defined the plasmonic area. The chips are be measured by conventional fiber-waveguide-fiber method as the conventional Si photonic chips.

The diced chips were measured using a fiber-to-fiber measurement setup. Quasi-TE-polarized light (for the MISIM nanoplasmonic waveguides) or Quasi-TM-polarized light (for the MIS hybrid plasmonic waveguides) is coupled into the input Si channel waveguide from a lensed polarization-maintaining (PM) single-mode fiber, transports through the waveguide, and then is coupled out to another fiber to be measured by a power meter and an optical spectrum analyzer (OSA). A semi-auto micrometer piezo-stage was used to adjust both input and output fibers to search the maximum output power.

Numerical simulation was performed using commercial software Lumerical™. The refractive indices of Si_3N_4 and SiO_2 are set to 2.0 and 1.444, respectively, and the complex index of Cu at 1550 nm is set to $0.282 + j11.05$.

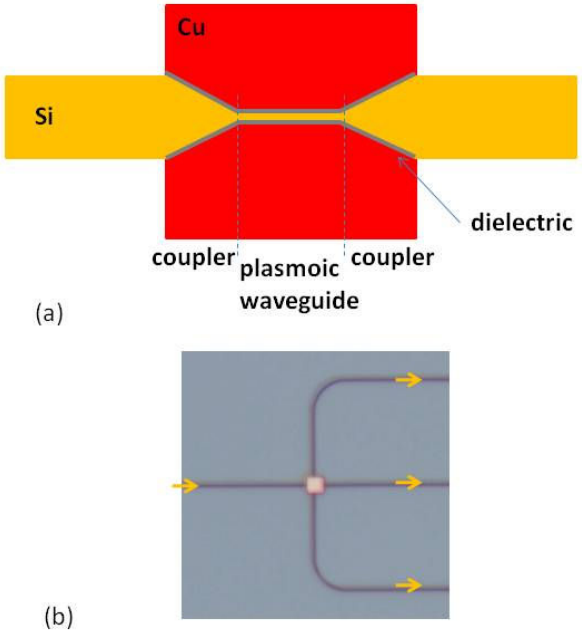

Fig. 3 (a) Schematic layout of plasmonic waveguide (as well as plasmonic waveguide based devices) inserted in conventional Si channel waveguide. A tapered coupler can reduce the coupling loss between the plasmonic waveguide and the conventional Si waveguide, (b) photography of the final chip, the Cu-covered area is defined the plasmonic area

III. Results and Discussion

The differences between these two plasmonic waveguides are investigated both theoretically and experimentally. Because the SPP excitation requires the electric field of optical mode perpendicular to the metal/dielectric interface, the MISIM nanoplasmonic waveguides support transverse electric (TE)-polarized light while the MIS hybrid plasmonic waveguides support transverse magnetic (TM)-polarized light. Besides this obvious difference, we can see that the MISIM nanoplasmonic waveguides can confine the optical mode more tightly than the MIS hybrid plasmonic waveguides. As a result, the MISIM nanoplasmonic waveguides exhibit larger propagation loss than the MIS hybrid plasmonic waveguides. Fig. 4 shows the measured output power on straight plasmonic waveguides with different length (L_P), normalized by that measured on the corresponding reference Si channel waveguide without the plasmonic area. For both kinds of plasmonic waveguides, we can see that the output power depends on L_P almost linearly, from which, the propagation loss can be extracted. For example, a Cu-SiO_2-Si-SiO_2-Cu nanoplasmonic waveguide with ~21-nm-wide Si core and ~12-nm-thick SiO_2 exhibits propagation loss of ~0.63 dB/μm, and a Cu-SiO_2-Si hybrid plasmonic waveguide with ~160-nm×304-nm Si core and ~20-nm-thick SiO_2 exhibits propagation loss of ~0.12 dB/μm.

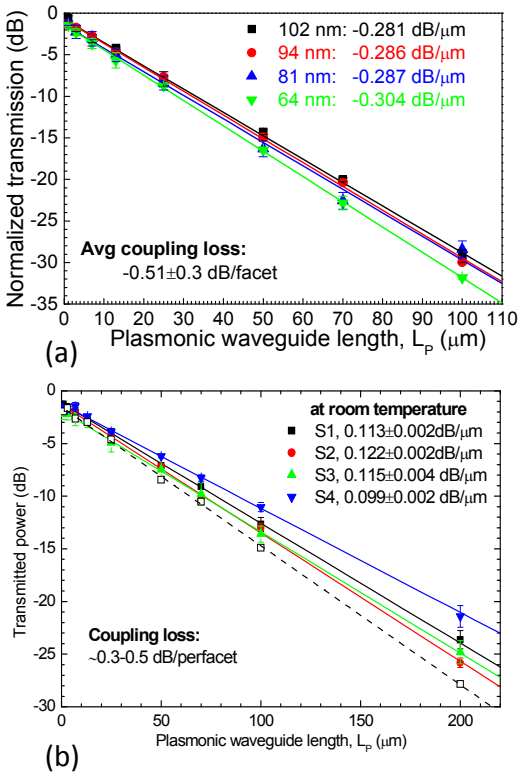

Fig. 4 Measured output power measured on straight plasmonic waveguide versus the plasmonic waveguide length, normalized by that measured on the reference Si waveguide without the plasmonic area: (a) MISIM nanoplasmonic waveguide, and (b) MIS hybrid plasmonic waveguide

Various passive devices, including ultracompact bends, power splitters, Mach-Zehnder interferometers, waveguide-ring resonators, TE/TM splitters, and polarization rotators have been experimentally demonstrated based on the above two plasmonic waveguides using standard CMOS technology. In general, the MISIM plasmonic waveguides support sharp bending with lower bending loss owing to the tight optical mode confinement as compared with the MIS hybrid plasmonic waveguides, while the MIS hybrid plasmonic waveguides support evanescent coupling as the conventional dielectric waveguides, thus enabling to realize waveguide-ring resonators with relatively large quality factor. Fig. 5 shows the schematic layout of the plasmonic ring resonators. The straight bus plasmonic waveguide has length of 7μm and width (W_P) of 0.18μm, which is linked with input/output 0.5-μm-wide Si strip waveguides through 1-μm-long tapered couplers. A microring adjacent to the bus waveguide has the same width of 0.18μm and the central radius (R) of 2.59μm. The separation gap between the ring and bus waveguide is 0.2μm. Fig. 5 (c) is a SEM image of the Si core of the fabricated plasmonic ring resonator. Fig. 5 (d) is the transmission spectrum measured on the resonator, normalized by that measured on the corresponding 7-μm-long straight plasmonic waveguide. One sees that it exhibits quality factor of ~275 and extinction ratio of ~12.8 dB.

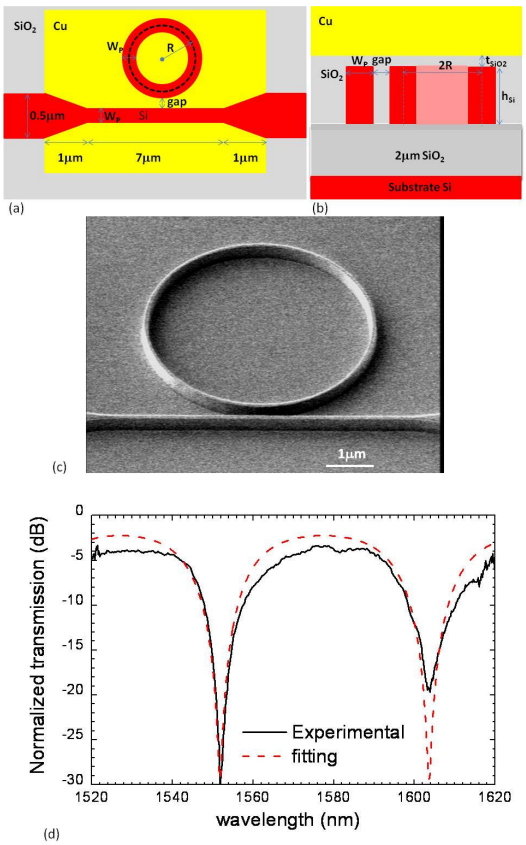

Fig. 5 The Cu-SiO_2-Si hybrid plasmonic waveguide-based WRRs: (a) Schematic layout, (b) Cross section, (c) SEM image of the patterned Si core of a typical WRR with R of 2.59μm, and (d) The measured transmission spectrum, normalized by that measured on corresponding 7-μm-long straight plasmonic waveguide

The plasmonic modulators have also been demonstrated based on these two plasmonic waveguides, which rely on the voltage induced electron accumulation at the dielectric/Si interface. With the concentration of accumulated electrons increasing, the real part of Si refractive index decreases and the imaginary part increases. The real part of Si refractive index can be close or even smaller than the dielectric refractive index if the electron concentration in the accumulation layer is high enough (e.g., ~6×10^{20}cm^{-3}), thus the optical mode will be mostly confined in this narrow (~1 nm) accumulation layer, which in turn modulate the effective modal index (both the real and imaginary parts) of the plasmonic waveguides, as shown in Fig. 6. Electro-absorption and phase modulators with ultracompact size (e.g., ~3μm long) have been experimentally demonstrated, as shown in Fig. 7.

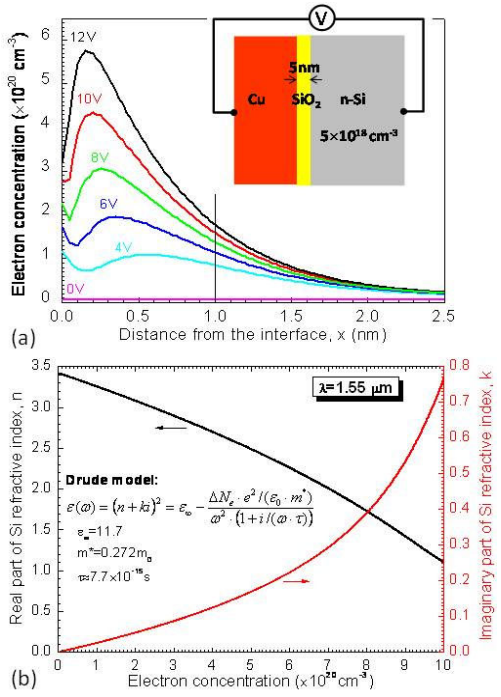

Fig. 6 (a) Spatial electron distribution in a Cu/5-nm-SiO_2/n-Si capacitor, as shown schematically in inset, under different voltages, obtained from 1-D MEDICI simulation; and (b) Real part (n) and imaginary part (k) of Si complex index as a function of free electron concentration based on the Drude model

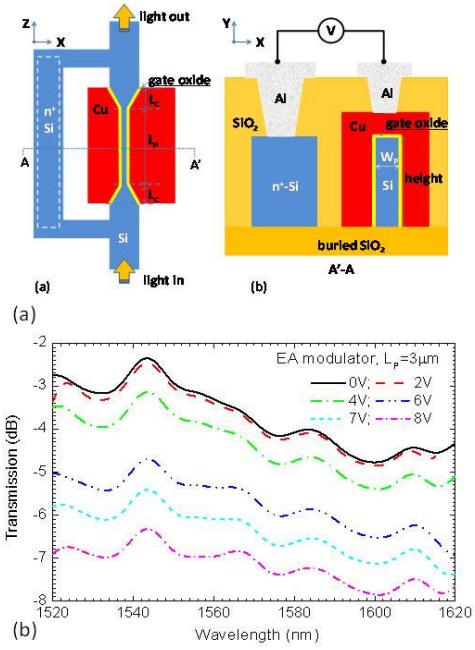

Fig. 7 (a) Schematic of a proof-of-concept Si plasmonic modulator based on the horizontal MISIM plasmonic waveguide: (a) top view and (b) cross-sectional view along A-A', and (b) Transmission spectra measured on an EA modulator with 3-μm L_P under voltage ranging from 0 to 8V, normalized by the spectrum measured on a reference Si waveguide without the plasmonic structure

IV. Conclusion

Two CMOS-compatible plasmonic waveguide platforms are developed as horizontal Cu-insulator-Si-insulator-Cu nanoplasmonic waveguide and vertical Cu-insulator-Si hybrid plasmonic waveguide. Various passive and active plasmonic devices are demonstrated based on these two platforms using standard CMOS technology. Although the performance of the demonstrated ultra-compact plasmonic modulators is not good at this stage, it can be significantly improved as predicted theoretically (i.e., up to 100 GHz, which is difficult for conventional Si modulators).

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