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14-Bit 1MS/s Cyclic-Pipelined ADC

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***Abstract*—**This paper presents a 14-bit cyclic-pipelined Analog to digital converter (ADC) running at 1 MS/s. The architecture is based on a 1.5-bit per stage structure utilizing digital correction for each stage. The ADC consists of two 1.5-bit stages, one shift register delay line, and digital error correction logic. Inside each 1.5-bit stage, there is one gain-boosting op-amp and two comparators. The ADC was implemented in 0.18μm CMOS process and the design has an area of approximately 0.2mm^2. The ADC has a differential input range of 1.2 Vpp. The circuit has an average power consumption of 3.5mA with 10MHz sampling clocks. The post-layout simulations of the design satisfy 12-bit SNDR with a full-scale sinusoid input.

***Keywords*—**Analog to digital converter, cyclic, gain-boosting, pipelined.

I. Introduction

ELECTRONIC applications like ultrasonic medical imaging, digital video and wireless transceivers require high resolution (10-14 bits) analog to digital converters (ADCs) with moderate speeds (1-10MS/s). ADCs are one of the key components in these systems for converting the analog quantities to digital data for information processing, data transmission and control. The technology scaling results in lower supply voltage, smaller devices, resulting in faster operation and lower power which makes the design of high resolution ADCs challenging. Successive Approximation ADCs have good energy efficiency and its simple analog architecture make it suitable for nanometer CMOS technologies [3]. But the SAR ADCs are limited in speed. The resolution depends on the comparator noise and the capacitor matching that can be obtained in the process [1]. Even moderate resolution ADCs require huge input capacitance for good matching [2], [5]. This makes them unsuitable for high speed which needs smaller capacitance and faster settling. Sigma-delta ADCS are good for applications that need low speed and high resolution. For systems that need high speed the preferred architectures are flash and pipelined ADCs. Flash converters are suitable for high speed but they are very power hungry for high resolutions. The number of comparators double for every additional bit of resolution required.

Pipelined A/D conversion has several advantages over more traditional flash converters. The main advantage is that pipeline converters have much lower power consumption because the number of comparators increases linearly with bit resolution. The pipeline architecture because of its high tolerance of process variations, low power consumption, and smaller area make them very attractive for system level integration.

The design of ADCs is an evolving field with various new architectures coming up. New architectures take advantage by combining two standard architectures to obtain a better ADC. The paper [3] shows a SAR assisted pipelined architecture that uses a two stage pipelined ADC along with a SAR based sub-ADC to obtain a 12-bit ADC.

Despite the advantages offered by the pipelined ADC a standard 1.5-bit per stage pipelined architecture needs N op-amps and 2N comparators for N bit resolution. This results in increased area, power and complexity. In applications that require moderate speeds of about 1-10MS/s and those in which the data latency is not critical we can reuse the pipeline stages in a cyclic fashion. This technique can reduce the numbers of pipeline stages required to obtain the required resolution. This architecture though limits the speed but improves the area and power required for a given resolution. The total analog hardware used is minimized. This paper presents an ADC that uses this technique to obtain a cyclic-pipelined ADC that has two 1.5-bit pipeline stages to obtain a resolution of 14 bits.

The detailed architecture of the ADC and the description of the various blocks are given in the section II. Section III covers the simulation results of the ADC. Section IV concludes with a summary.

II. Architecture

The architecture is based on a 1.5-bit per stage structure utilizing digital correction for each stage. There are only two 1.5-bit pipeline stages as shown in Fig. 1.

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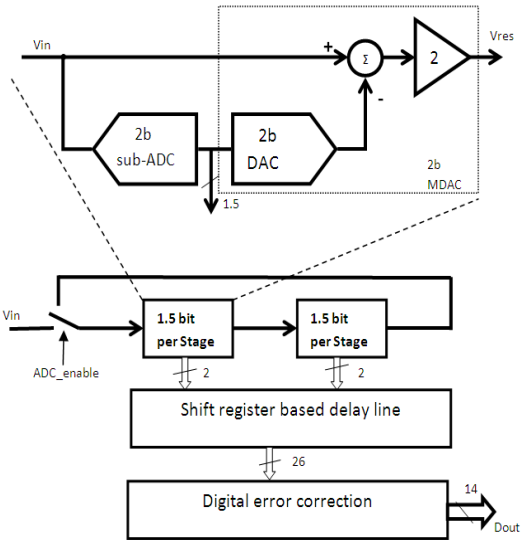

Fig. 1 Cyclic-pipelined ADC Architecture

A differential switched capacitor circuit consisting of a gain-boosting op-amp with 360MHz unity-gain bandwidth is used for sampling and amplification in each stage. Differential dynamic comparators are used to implement the decision levels required for the 1.5-bit per stage structure. Each stage has a gain boosting op-amp and two comparators. The ADC operates just like a SAR ADC with the difference that each cycle effectively resolves two bits. The ADC samples the input data for 3 cycles. The residual of the first stage is quantized by the second stage. The two stages resolve two bits per cycle of clock and the residual of the second stage was fed to the first stage again. In this way, the analog signals loop in the two pipeline stages. The ADC requires 7 conversion clock cycles to obtain 14-bit data. Since the bits are generated at different times there is a digital shift register block that synchronizes the data. This block aligns the bits obtain in each clock cycle properly and then the result is fed to the digital correction circuit that consists D-Flip-Flop and full-adders which provides the final 14-bit data.

A. First Pipeline Stage

The first pipelined stage as shown in Fig. 1 consists of a 2-bit MDAC and Sub-ADC. During each conversion, the input signal was sampled by the MDAC. At the same time, the input signal was also quantized by the two comparators inside the sub-ADC. Then, a constant voltage, +Vref/4 or 0 or –Vref/4 was subtracted from the input signal in MDAC and the residue was amplified by 2 and fed to the next stage. The MDAC is a switched-capacitor circuit which employs CDS technique to remove op-amp 1/f noise and offset voltage.

To guarantee a 14-bit accuracy, the op-amp used in MDAC has gain-boosting stages to boost the open-loop gain of op-amp up above 110dB. The sample and hold circuit speed and linearity are determined by the settling time required for the op-amp. The unity gain bandwidth (ωu) of the op-amp is directly related to resolution (N) of the ADC and this as given by (1).

$$\omega u > 2(N+1).fs.\ln 2/\beta \quad (1)$$

where fs is the sampling frequency of the ADC and β is the feedback factor [4]. Normally the op-amp has to be designed with a unity gain band with larger than this to take into account the non over lapping clock phases and slewing of op-amp [4].

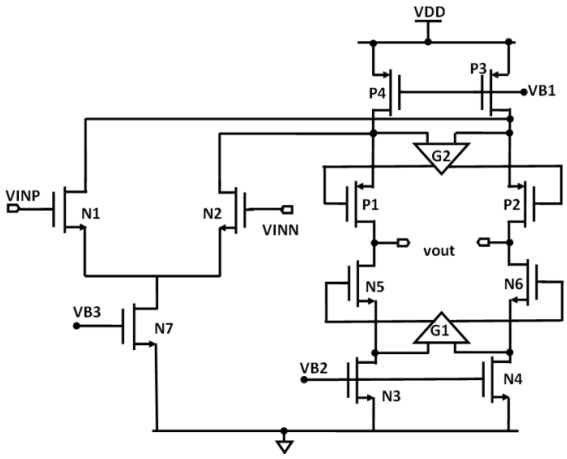

Fig. 2 Gain boosting op-amp

The gain-boosting single-stage op-amp shown in Fig. 2 provides high voltage gain and also increases the output swing. Furthermore NMOS transistors are used as input devices while PMOS as cascade transistors in order to get low power dissipation, high voltage gain, higher pole frequencies (better stability). A switched-capacitor common-mode feedback (CMFB) network was added to sense the common-mode level of the two outputs and accordingly adjust the bias current in the op-amp.

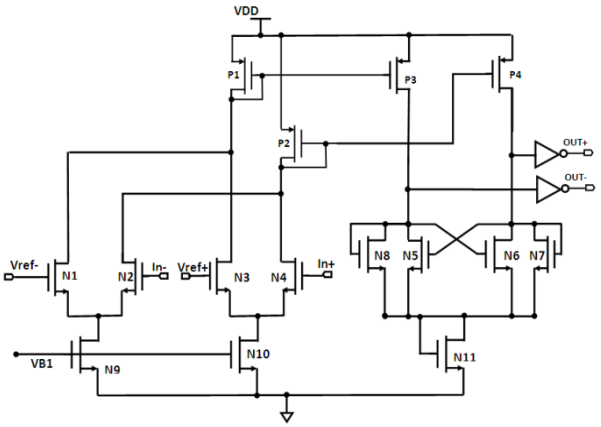

Fig. 3 Differential comparator

The comparator used in the sub-ADC block is shown in Fig. 3. It has a pre-amp stage to reduce the kick-back noise and a cross-coupled second stage to improve the regeneration time.

Since the operation of the comparators is differential the references can simply be inverted for the second comparator. Logic in the sub-ADC block receives the output from the comparators and generates the control signal for the switches in the MDAC block and provides the digital outputs to the shift register block.

B. Second Pipeline Stage

The second pipeline stage is similar to the first stage except that it does not sample the analog input signal directly. The residue from this stage is fed back as input to the first stage.

C. Non Overlapping Clock Generation

An MDAC stage requires non-overlapping clocks to define its sample and hold phases. This is generated by a chain of inverters driving MOS capacitors. The non-overlapping time was controlled by the MOS capacitors.

D. Shift Register and Digital Error Correction

The two stages of pipeline provides 4 bits every cycle and the 26 bits generated (2 bits are discarded) are fed to the shift register delay line. Because of the delays inherent in a pipeline architecture MSB bits are provided a few clock cycles before the LSB. To align the bits in time, a shift register works as a delay circuit. This data is then fed to the digital error correction circuit.

Errors caused by offsets in the comparator can be cancelled out by using digital error correction logic. The extent to which comparator errors can be cancelled depends on number of bits each pipeline stage is designed to resolve. In the case of a 1.5-bit per stage architecture, comparator offsets up to ¼ VFS can be effectively handled. An error occurs when the next stage cannot properly convert an out-of-range signal. Without using digital correction, the output bits are not useful. The digital error correction consists of full adders and it corrects the 26 - bit data with redundancy to give the 14-bit digital output data.

III. Simulation Results

The 14-bit 1MS/s cyclic-pipelined ADC for 1.2V peak to peak differential input was designed under 0.18um CMOS process. The layout of ADC is shown in Fig. 4. The active area of the ADC is about 500um x 400um.The bulk of the area is occupied by the analog portion of the ADC.

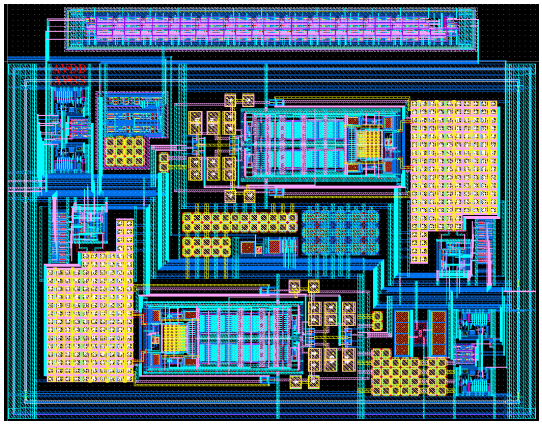

Fig. 4 Layout of the ADC test chip

The simulation result of the ADC with a 3kHz, 1.2V peak to peak differential input signal at an output data rate of 1MS/s depicted in Fig. 5 demonstrates that the ADC can achieve a SNDR of 81dB that corresponds to an ENOB of 13.1 bits. The SFDR in was also greater than 85dBc.

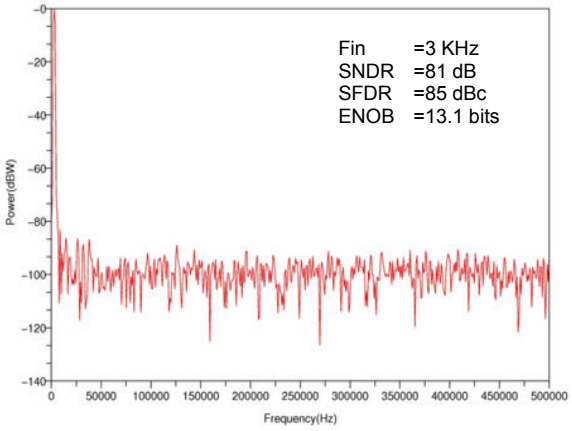

Fig. 5 Spectral plot of the ADC output

The post layout of the ADC also showed that it can achieve an ENOB of 12-bits. With an input close to the Nyquist frequency the ADC can achieve close to 11-bits of ENOB. The ADC consumes about 3.5mA of current of which the analog block consumes about 3.3mA and the digital blocks consume about 200uA of current. The total power consumption of the chip is about 6.3mW of power.

IV. Conclusion

A 14-bit, 1MS/s cyclic-pipelined ADC has been designed and fabricated in 0.18µm technology .The ADC occupies an active area of 0.2mm^2. With just two pipeline stages the ADC is able to obtain 14-bit resolution resulting in area saving. The ADC achieves more than 13-bit ENOB in simulations with a 1.2V peak to peak differential input. It consumes about 6.3mW of power with a 10 MHz input clock. It can also achieve a good SFDR of about 85dBc.

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