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Electrical Characterization and Reliability Analysis of HfO2-TiO2-Al MOSCAPs

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***Abstract*—** MOSCAPs of various combinations of Hafnium oxide and Titanium oxide of varying thickness with Aluminum as gate electrode have been fabricated and electrically characterized. The effects of voltage stress on the I-V characteristics for prolonged time durations have been studied and compared. Results showed hard breakdown and negligible degradation of reliability under stress.

***Keywords*—** breakdown, MOSCAP, voltage stress.

I. Introduction

THE aggressive scaling of CMOS devices for high speed and low power applications has led to technology nodes smaller than 65nm.This has led to scaling of gate dielectric to very small dimensions. SiO_2 as thin as 1.2nm has already been successfully implemented in the 90nm technology node [1]. Research transistors with 0.8nm SiO_2 have also been demonstrated in the laboratory [2]. However, continued gate dielectric scaling will result in large tunnelling leakage current through the thin layer of dielectric. Another problem is caused by the long term use of the chip at elevated temperature which causes breakage of bonds at Si/SiO2 interface leading to trapped oxide charges as well as a Vt shift which affects the reliability [3]. So, in order to continue the scaling of gate dielectric further, we need to use high-K material, as SiO2 will eventually run out of atoms for further scaling.

To reduce all the above mentioned problems associated with SiO2, we use high k dielectrics. The basic requirement for any alternative to SiO2 is that it should have good thermal stability in contact with Si preventing formation of thick SiOx interfacial layer and formation of silicide layer. It should also possess low density of intrinsic defects at the Si/dielectric interface and in bulk providing high mobility charge carriers in the channel and sufficient gate dielectric lifetime. Any dielectric replacing SiO2 should have large energy band gap providing high energy barriers at the Si/dielectric and metal gate/dielectric interface in order to reduce the leakage current flowing through the structure. It also should have high crystallization temperature [4].

By using HfO2 (K ~ 20), or TiO2 (K ~ 40), we can replace a 1nm SiO2 film with a 5nm HfO2 or a 10nm TiO2 film, thereby reducing tunneling leakage current significantly. HfO2 provides a much thicker barrier considerably reducing the effect of tunnelling and in turn the problem of leakage current. Therefore, it will be able to provide a good interface with the silicon substrate. It is well known that HfO2 and TiO2 are potential candidates for continued scaling MOS devices. So, a stack combination of HfO2 at the interface followed by a thin layer of TiO2 promises exciting results.

In this paper, we present the characteristics of various combinations of HfO2-TiO2-Al gate stacks. The thicknesses of both the dielectric layers have been varied. Also, different predeposition treatments on the silicon surface were carried out.

II. Device Fabrication Process

The process flow for various high k MOSCAPs with HfO2/TiO2/Al stacks is summarised in Table1. Two types of pretreatment have been performed: one with RCA cleaning and HF last and the other with RCA cleaning and HF last followed by a forming gas anneal (600C for 40 seconds). HfO2 was deposited using MOCVD (400C for 6-8 seconds, Precursor flow: 20MGM, O2 flow: 1000 sccm) and TiO2 by sputtering Ti first (150W, 12-18 seconds) followed by RTP oxidation. Aluminum gate was deposited on top by evaporation using shadow mask. Subsequently, a high temperature anneal was performed in N2 ambient (700C for 60 seconds).

I-V and stress I-V curves were measured using Keithley 4200 SCS fully shielded probe station with triax chuck. Thicknesses were measured using spectroscopic ellipsometer.

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III. Results And Discussion

The I-V and stress I-V characteristics of the fabricated MOSCAPs were measured. The effective breakdown field of HfO2-TiO2-Al devices ranged from 4-6 MV/cm. The samples have negligible Coulomb scattering centers such as interface state charges and charges trapped in oxide under constant voltage stress as can be observed from the stress I-V graphs. Also, Stress Induced Leakage Current (SILC) was not significant. In conclusion, the fabricated devices have showed good stability and reliability.

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TABLE I
Process Flows For Different Gate Stack Combinations

Process Step	Process Flow I	Process Flow II	Process Flow III
Pretreatment	RCA and HF Last	RCA and HF Last followed by Forming Gas anneal @ 600C for 40 seconds	RCA and HF Last followed by Forming Gas anneal @ 600C for 40 seconds
Bottom Dielectric	HfO2 (Thickness: 4.5 nm)	HfO2 (Thickness: 3.5 nm)	HfO2 (Thickness: 3.5 nm)
Top Dielectric	TiO2 (Thickness: 4.0 nm)	TiO2 (Thickness: 4.0 nm)	TiO2 (Thickness: 4.4 nm)
Post Deposition Anneal	700C in N2 for 60 sec	700C in N2 for 60 sec	700C in N2 for 60 sec
Total Dielectric Thickness	8.5 nm	7.5 nm	7.9 nm
Breakdown Field	5.47 MV/cm	5.60 MV/cm	4.68 MV/cm

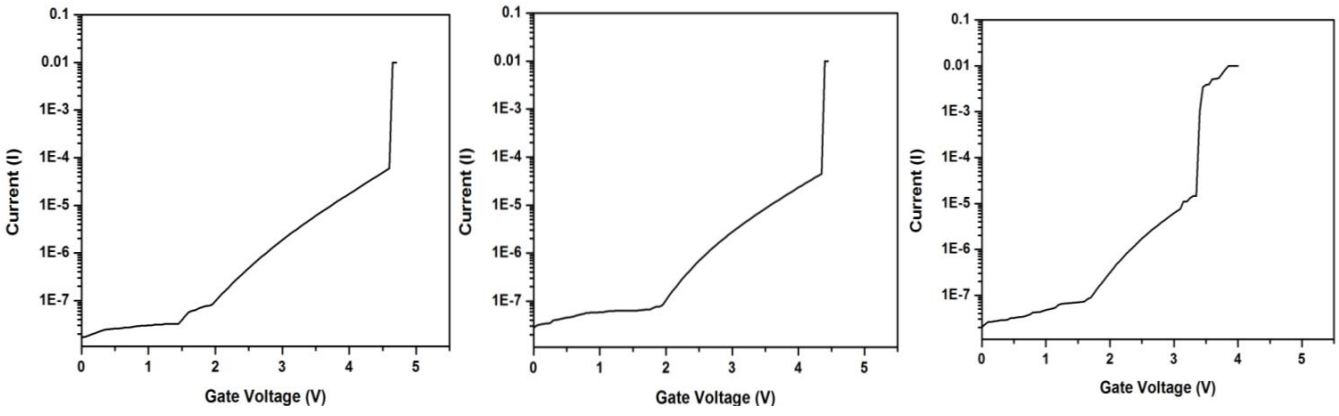

Fig. 1(a) Fig. 1(b) Fig. 1(c)

Fig. 1. I-V Characteristics of MOSCAPs (a) Process Flow I (b) Process Flow II (c) Process Flow III

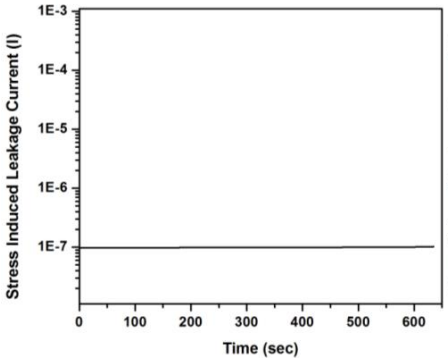

Fig. 2(a)

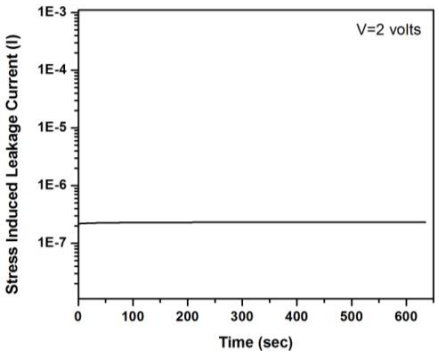

Fig. 2(b)

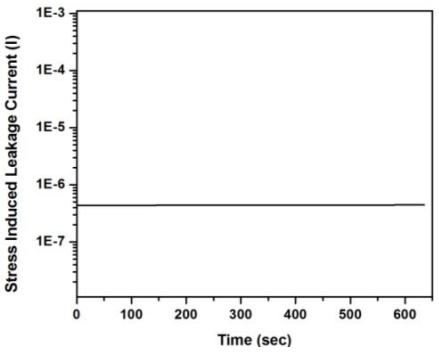

Fig. 2(c)

Fig. 2. Stress Induced Leakage Current Characteristics of MOSCAPs at 2 volts for 630 seconds (a) Process Flow I (b) Process Flow II (c) Process Flow III

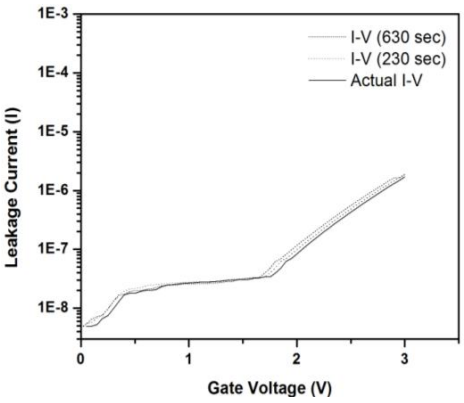

Fig. 3(a)

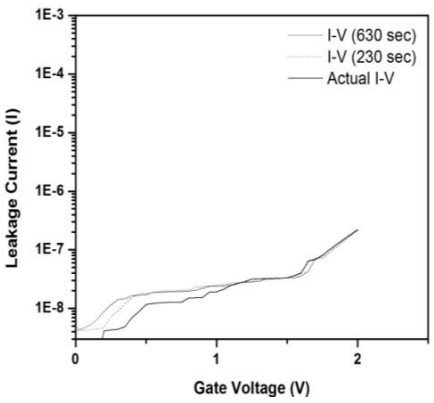

Fig. 3(b)

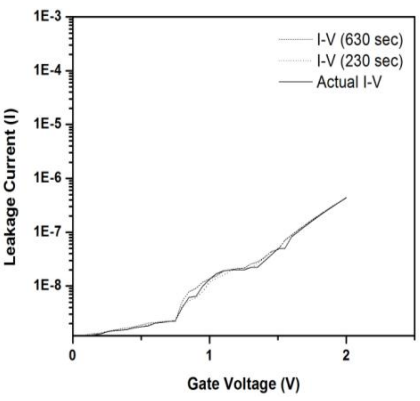

Fig. 3(c)

Fig. 3. Stress IV Analysis: Stress of 2 volts applied for different time durations compared against the unstressed condition (a) Process Flow I (b) Process Flow II (c) Process Flow III