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Thermal Stability of a Vertical SOI-Based Capacitorless One-Transistor DRAM with Trench-Body Structure

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***Abstract*—**A vertical SOI-based MOSFET with trench body structure operated as 1T DRAM cell at various temperatures has been studied and investigated. Different operation temperatures are assigned for the device for its performance comparison, thus the thermal stability is carefully evaluated for the future memory device applications. Based on the simulation, the vertical SOI-based MOSFET with trench body structure demonstrates the electrical characteristics properly and possess conspicuous kink effect at various operation temperatures. Transient characteristics were also performed to prove that its programming window values and retention time behaviors are acceptable when the new 1T DRAM cell is operated at high operation temperature.

***Keywords*—**SOI, 1T DRAM, thermal stability.

I. Introduction

RECENTLY, the experimental and simulation results on the performance of capacitorless 1T DRAM show that using an additional body layer as the charge storage region has been carried out and considered as a competitive candidate for future memory device [1]-[5]. However, the conventional planar-type PDSOI 1T DRAM cell meets the same huge barriers as traditional DRAM had, that is the shorten retention time behavior caused by the reduced charge storage region for hole saving [6]-[9]. To solve the above issues, a TFT-based 1T DRAM device with trench body structure was proposed to improve the transient performance [10], [11]. However, the misalignment fabrication steps seriously impact the device performance, and the reduced device size also leads to a limited charge storage region for holes. Therefore, we proposed a vertical SOI-based MOSFET to overcome the above issues and served as a 1T DRAM cell successfully as shown in Fig. 1 [12]. In this study, we investigate the thermal stability of the vertical SOI-based MOSFET operates as the 1T DRAM cell at various temperatures. Because of the additional trench body region underneath the device, the heat can not only accumulate in the channel region, but also spread out to the trench body region. Thus, the self-heating effects (SHEs) are suppressed and the electrical characteristics and transient performance are improved at higher operation temperature.

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II. Simulation Setup

In this study, we use the ISE-TCAD 2-D simulation tool FLOOPS [13] to simulated the vertical SOI-based 1T DRAM cell with gate length (L_G) of 48 nm for performance comparison at different operation temperature.

The simulation results will show in the next chapter. For simulation, the Hydrodynamic transport model is used to calculate the device drift-diffusion for transport in all simulations. The Shockley-Read-Hold (SRH) and Auger Avalanche (CarrierTempDrive) models are used for the calculating the device generation-recombination behavior. As for the interface phenomena, the model named High Field Saturation (CarrierTempDrive), PhuMob, and Enormal are used in the simulations. For the density gradient quantum correction, the model eQuantumPotential and hQuantumPotential are switched on. For the interface traps definition, the MaterialInterface model is switched on.

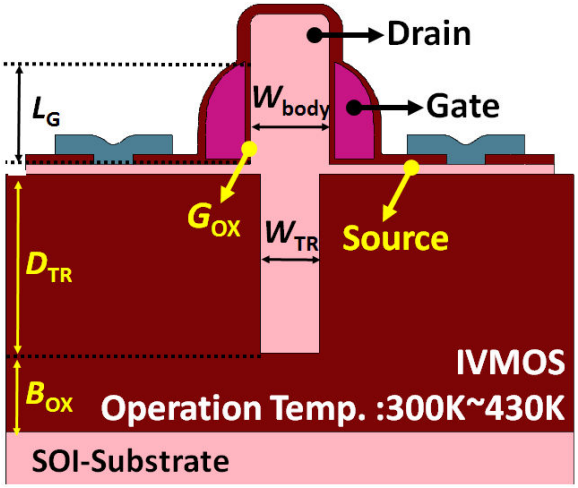

Fig. 1 The device structure of the vertical SOI-based 1T DRAM cell with trench body region

TABLE I
Device Parameter of the Proposed IVMOS

Device Parameter	
Gate Length, L_G	48 nm
Gate Oxide, G_{OX}	3 nm
Trench Width, W_{TR}	30 nm
Trench Depth, D_{TR}	90 nm
Channel Body Width, W_{body}	40 nm
Source Thickness, T_S	5 nm
Buried Oxide, B_{OX}	40 nm

II. Simulation Results

To clarify how the operation temperature affects the device electrical characteristics and transient performance, Fig. 2 shows the I_D-V_G characteristics of the vertical SOI-based 1T DRAM cell with gate length (L_G) of 48nm, and the device operates in different room temperature of 300K, 330K, 373K, and 430K for performance comparison. We can clearly show that the device on-state current is degraded when the device operation temperature is increased. And, the off-state leakage current is increased as the temperature goes higher. This is because the higher operation temperature will lower the device thermal stability and shorten the device lifetime. Nevertheless, we found out that the proposed device can achieve the I_{ON}-I_{OFF} current ratio performance higher than 10^3 even when the device operates in 430K. This is because the trench body region can act as an additional body region and shares the heat, hence improves the device behavior when the device works in a higher operation temperature.

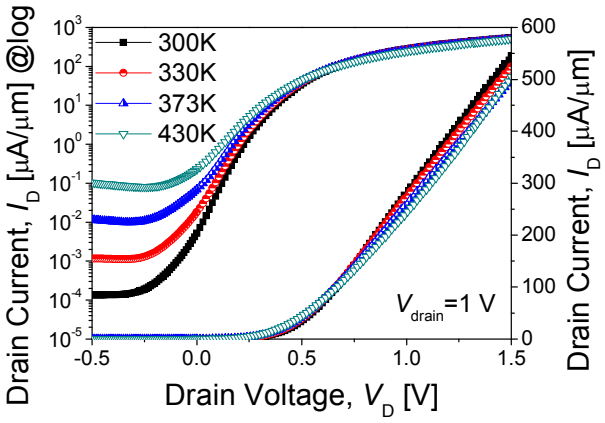

Fig. 2 Simulated I_D-V_G curves for the device with 48 nm gate length

Fig. 3 shows the I_D-V_D characteristics of the proposed VSOI-based device. It can be observed that the floating-body effects (FBEs) are degraded as the operation temperature is increased. The reason is that the higher temperature will lower the encroachment of the drain, and thus suppresses the kink effect occurred and lowers the DIBL (as shown in Fig. 4). Also, the higher operation temperature will decrease the drain current value. Fortunately, the device can still maintain an obvious kink effect when operates at 430K and achieve an available drain current characteristic with only 32% lower than the device does at 300K.

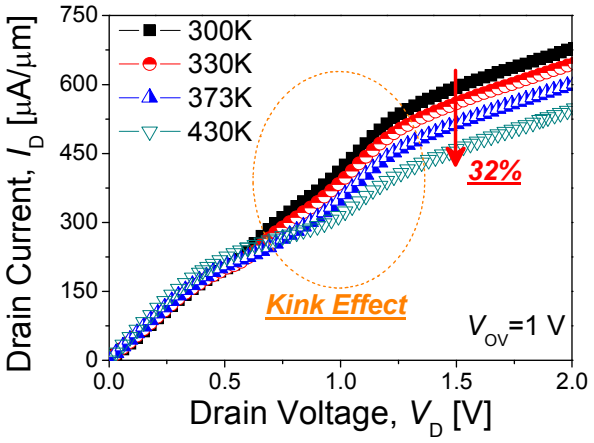

Fig. 3 Simulated I_D-V_D curves for the device with 48nm gate length

Fig. 4 shows the drain induced barrier lowering (DIBL) and subthreshold swing (S.S.) properties as function of device operation temperature for the vertical SOI-based 1T DRAM cell. It is interesting that the DIBL value is decreased as the operation temperature goes higher. It is because the higher operation temperature makes the device lower its kink effect, hence the encroachment of the drain is decreased and the DIBL is decreased. On the other hand, the I_{ON}-I_{OFF} current ratio is reduced at higher temperature, thus lowering the subthreshold swing properties.

In order to clarify how the operation temperature affects the device transient characteristics, Fig. 5 shows the completed drain current properties as function of time for the IVMOS operating at various operation temperatures. We can clearly see that the proposed IVMOS can serve as a 1T DRAM cell successfully during write, read, and hold process. Meanwhile, we also found out that the read "1" drain current is decreased and the read "0" drain current is larger as the temperature is increased (as shown in Fig. 6) thereby leading to a smaller programming window properties. Fortunately, the results are still acceptable with the device programming window of 33.5μA/μm for the 430K one.

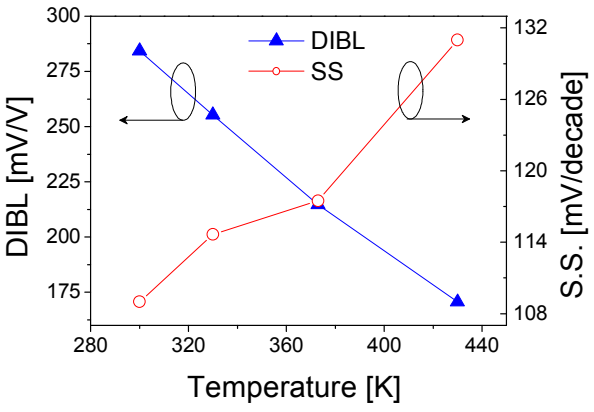

Fig. 4 Simulated drain induced barrier lowering (DIBL) and subthreshold swing (S.S.) characteristics for the device with 48nm gate length

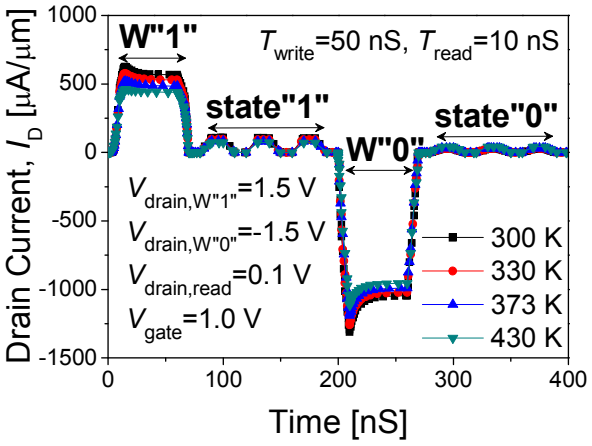

Fig. 5 Simulated transient characteristics for the proposed 1T DRAM cell

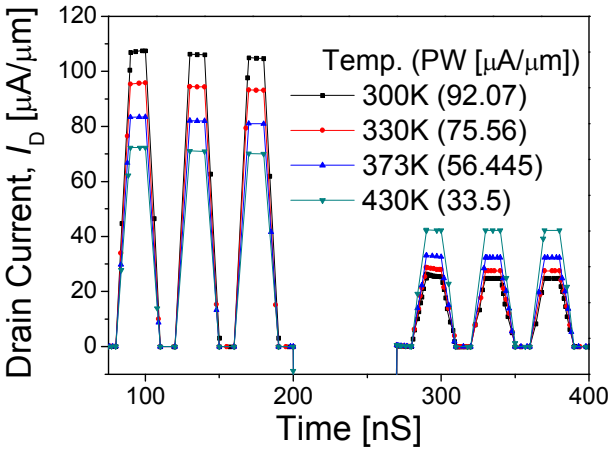

Fig. 6 Simulated programming window properties for the proposed 1T DRAM cell

Fig. 7 shows the transient characteristics during write "1" process. It is interesting that the write "1" time of the device show similar results at various temperatures. In fact, the time for the write "1" process at 430K is only 11% longer than that of the device operates at 300K. This is because the trench depth and the drain electric field are on the same downward direction, thus the drain electric field can easily affect the charge storage region in a short time at various temperature.

Fig. 8 shows the programming window as function of write "0" drain voltage ($V_{write"0"}$) for the proposed 1T DRAM cell at various operation temperatures. It can be clearly seen that the proposed device achieves a large programming window larger than 50μA/μm when the operation temperature lower than 373 K. We also found out that the characteristic trends for different operation temperature are different. We know that a larger $V_{write"0"}$ will help erase the charge store in the trench body region and receive a larger programming window value. However, a larger $V_{write"0"}$ will also cause the self-heating effects (SHEs) occurred. Nevertheless, an interesting results of 430 K shows that the lower $V_{write"0"}$ receive larger programming window value of 38.7 μA/μm at $V_{write"0"}$ = -1.2 V. This is because the reduced $V_{write"0"}$ suppress the SHEs, leading to a better programming window performance.

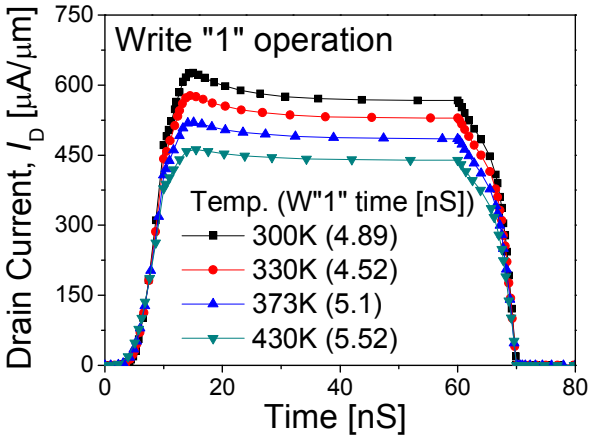

Fig. 7 Simulated transient characteristics during write "1" operation for the proposed 1T DRAM cell

Fig. 9 shows the retention time characteristics as function of Vwrite"0" of the VSOI-based 1T DRAM cell at various operation temperatures. The retention time is defined when the programming window value is smaller than 1μA/cell (15.625μA/μm) [12]. The results show that the device at 300K has better retention time properties. This means that the charge can be stored in the trench body region during write "1" process, and can also be erased by the negative drain bias during write "0" process successfully. However, a reduced retention time behavior occurs when the operation temperature is increased. This is because the higher operation temperature will increase the leakage current and recombination rate, thus shorten the retention time behavior.

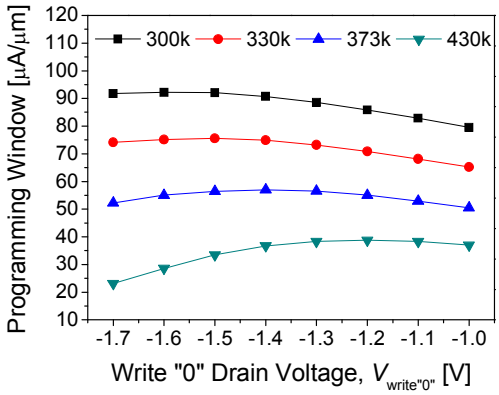

Fig. 8 Simulated programming window characteristics for the proposed 1T DRAM cell with various write "0" drain voltage ($V_{drain.}$ write"0")

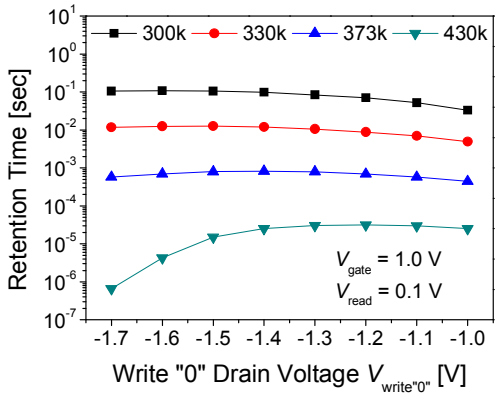

Fig. 9 Simulated retention time characteristics for the proposed 1T DRAM cell with various write "0" drain voltage $V_{drain.}$ write "0"

IV. Conclusion

We have investigated the vertical SOI-based 1T DRAM cell with trench body structure operating at various temperatures for thermal stability. The trench body structure used for functioning the 1T DRAM behavior under different temperature are also studied carefully A significant kink effect is shown due to the trench body region can served as a charge storage region perfectly even the device is operated at high operation temperatures. The proposed device maintains good electrical characteristics with I_{ON}-I_{OFF} greater than five orders and an acceptable retention time performance around 1mS at operation temperature of 373K. It is believed that the vertical SOI-based 1T DRAM cell with trench body structure allows for use in higher operation temperature situation on SOI substrate.

Acknowledgment

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