Design a Low Voltage- Low Offset Class AB Op-Amp

B.Gholami,S.Gholami,A.Forouzantabar,Sh.Bazyari

Abstract—A new design approach for three-stage operational amplifiers (op-amps) is proposed. It allows to actually implement a symmetrical push-pull class-AB amplifier output stage for well-established three-stage amplifiers using a feedforward transconductance stage. Compared with the conventional design practice, the proposed approach leads to a significant improvement of the symmetry between the positive and the negative op-amp step response, resulting in similar values of the positive/negative settling time. The new approach proves to be very useful in order to fully exploit the potentiality allowed by the op-amp in terms of speed performances. Design examples in a commercial 0.35-μm CMOS prove the effectiveness of theproposed strategy.

Keywords—Low-voltage op amp, design , optimum design

I. INTRODUCTION

THE cascade arrangement of three amplifier stages is becoming a more and more attractive solution to develop high-gain large-swing operational amplifiers (op-amps) in modern low-voltage CMOS technologies [1]-[6]. To guarantee the closed-loop stability of three-stage op-amps,a proper frequency compensation strategy is required. The simplest one is the well-known nested-Miller compensation (NMC) technique [7]. However, NMC amplifiers suffer from asignificant speed performance limitation [8]. Several strategies were proposed to improve the speed performances of three-stage op-amps by enhancing their bandwidth and slew rate. A convenient solution used in the most efficient three-stagetopologies is the introduction of a feedforward transconductance stage between the first stage and the output of the op-amp [5]-[12]. This stage allows the op-amp phase margin to be significantly improved by properly placing the zeros of the amplifier transfer function [8]. The addition of the feedforward stage in the amplifier topology results in a push-pull class-AB op-amp output stage whose maximum outputcurrent in both polarities is greater than the quiescent current. This allows the op-amp slewing performances to be significantly improved with respect to the simple NMC scheme [6]. In the most well-established design procedures for three-stage amplifiers, the transconductance of thefeedforward stage is typically set equal to the transconductance of the third amplifier stage aiming to have a symmetrical push-pull output stage [5]-[12].

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However,especially under large-signal conditions, this choice does not guarantee the actual symmetry of the op-amp ositive/negative step responses, leading to strong differences in the positive/negative op-amp settling times (namely t_{S+} and t_{S-},respectively) [9], [12]. This is a crucial issue, above all in a wide class of applications emanding for high-speed op-amps, such as switched-capacitor circuits and analog-to-digital onverters [1], [1], [13]. In these applications, the maximum system operating frequency is, in fact, basically determined by the worst among t_{S+} and t_{S-}. A strong difference between t_{S+} and t_{S-} directly results then in the impossibility of reaching themaximum speed potentially allowed by the op-amp (fixed by the best among t_{S+} and t_{S-}). In order to guarantee efficient designs by actually guaranteeing symmetrical positive/negative amplifier step responses, the large-signal settling behavior of three-stage op-amps is carefully analyzed and improved design guidelines are given in this work.

II. PROPOSED CIRCUIT

Fig. 1 shows a schematic diagram of the proposed rail-to-rail constant-g_m op amp, which consists of an input stage (M1-M14), an output stage (M15-M16) and a g_m-control circuit (M17-M31). The tail current of the p-channel differential pair is designed to equal that of the n-channel differential pair, i.e. $I_p \frac{1}{4} I_T$. M11-M12 and M13-M14 are the resistance loads for the n-channel and p-channel differential pairs, respectively. The common-gate amplifiers, M8 and M10, combine and amplify the signals of the comp-lementary differential pairs to the output stage [4]. The output stage is a complementary common-source amplifier.
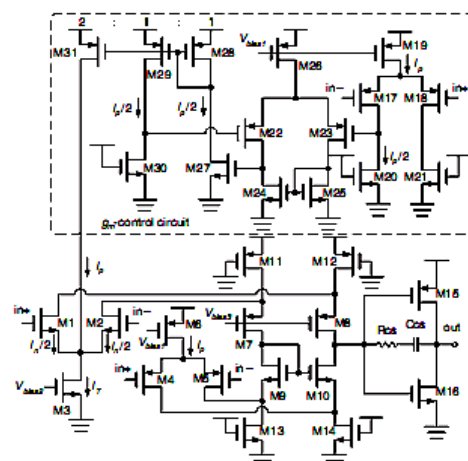

Fig. 1 Schemati diagram of proposed op-amp

The constant g_m is obtained by keeping the sum of currents in the complementary differential pairs constant rather than controlling the tail currents. The differential amplifier, constituted by M17-M21, is a replica of the p-channel differential amplifier, M4-M6 and M13-M14.Hence, the current flowing in the devices of these two amplifiers is equal. A negative feedback loop copies the currents in the replicate differential pair, M17-M18, to the devices, M27-M30. This negative feedback loop consists of a one-stage amplifier, M22-M26, and the current mirrors, M27-M30. By setting the sizes of M31 and M28 at a ratio of 2:1, a same value of the tail current, I_p , of the p-channel differential pair flows into the tail current source, M3, of the n-channel differential pair. The value of I_p depends on the input common-mode voltage (V_{icom}). The currents flowing in the n-channel differential pair can be expressed as:

$$I_n(V_{icm})=I_T-I_P(V_{icm})$$

When Vicom is in the low-level region, the current flowing in the p-channel differential pair, M4-M5, equals I_p. The same current value of I_p is also flowing in M3. This increases the voltage at the M1-M2 source node, and no current flows in M1-M2. The total current in the complementary differential is then I_T. If V_{icom} increases to the iff range, the currents in M4-M5 and M31 begin to reduce along with the M1-M2 source voltage. The currents in M1-M2 are then increased. However, the sum of currents in the complementary ifferent-tial pairs is maintained at a constant value of I_T. When V_{icom} urther increases to a higher level, no current flows in M4-M5, i.e. the value of I_p becomes zero. The total current in M1 and M2 then increases to the value of I_T. In summary, the currents in the n-channel differential pair are regulated to keep the sum of currents in the complementary differential pairs constant. Since the transconductance is proportional to the device current in the weak inversion, the total g_m of the first stage is constant over the input range.
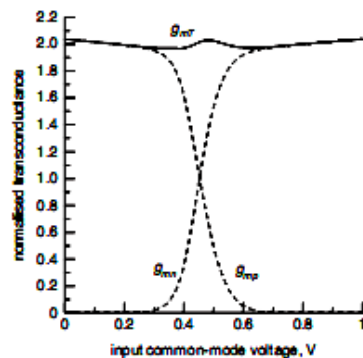

Fig.2 Simulated normalized amplifier transconductances against input common-mode voltage

III. PROPOSED DESIGN

The previously discussed asymmetry in the positive/negative op-amp step response directly comes from sizing the transistors of the amplifier output stage according to the conventional design criterion. In fact, it is worth pointing out that M_{10} and M_{11} are driven by two different signals in the op-amp of Fig. 2, V_{O2} being amplified with respect to V_{O1} by the gain of the second amplifier stage. Therefore, fixing the aspect ratio of M_{10} about three times larger than that of M_{11} in order to impose $g_{mf}=g_{m3}$ is not sufficient to actually guarantee a symmetrical push-pull class-AB output stage characterized by the same capability of charging/discharging C_L during the positive/negative op-amp step responses. To this aim, the aspect ratio of M_{10} should be instead further increased with respect to that of M_{11} in order to compensate also for the difference in the driving signals of the two transistors other than the different carrier mobilities. In other words, g_{mf} should be chosen sufficiently larger than g_{m3}

IV. SIMULATION RESULT

The proposed amplifier was simulated and fabricated using 0.35 mm CMOS technology. Fig. 2 shows the simulated normalised amplifier transconductances against V_{icom}. Variations in g_m lie within an error interval of +1.8%. The prototype test chip was connected as a unit-gain amplifier with a 1 V single power supply. The test chip was also loaded with a 55 pF capacitor.Fig. 3 shows the HSPICE simulation results for the op-amp designed according to theproposed approach: (a) positive/negative responses to a 500 mV-amplitude step; (b) op-amp output current.Fig.4 shows the HSPICE simulation results for the open-loop op-amp frequency response.
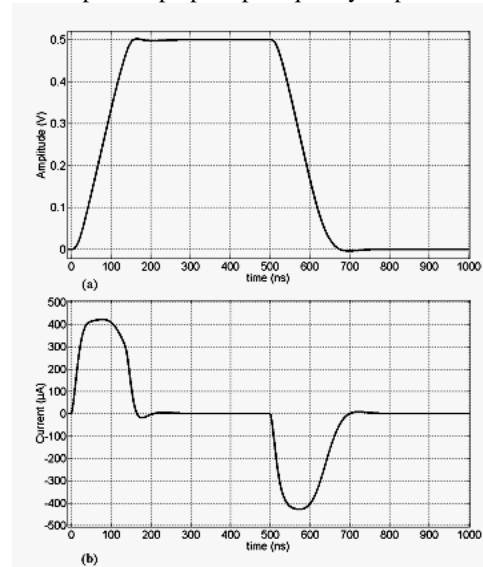

Fig. 3 HSPICE simulation results for the op-amp designed according to the proposed approach: (a) positive/negative responses to a 500 mV-amplitude step; (b) op-amp output current
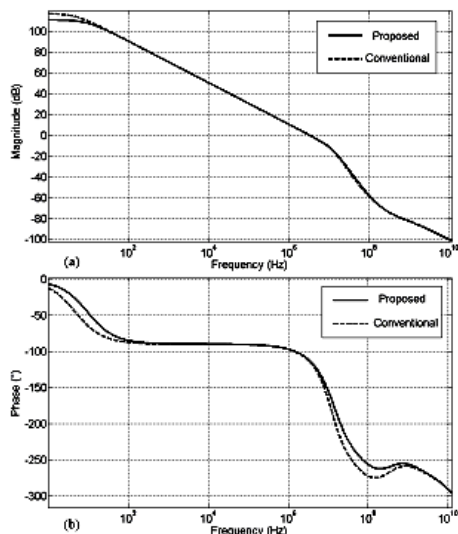
Fig.4 HSPICE simulation results for the open-loop op-amp frequency response: (a) Magnitude; (b) Phase

V. CONCLUSIONS

A new design approach for three-stage op-amps has been proposed. It is aimed to guarantee good settling performances for well-established three-stage amplifiers using a feedforward transconductance stage. On the contrary of conventional design criteria used for these op-amps, the proposed one actually allows to implement a symmetrical class-AB amplifier output stage. As shown by design examples in a commercial 0.35-μm CMOS technology, using the proposed design approach leads to a significant improvement of the symmetry between the positive and the negative op-amp step response, resulting in similar values of the positive/negative settling time. The new approach proves to be very useful in order to fully exploit the potentiality allowed by the op-amp in terms of speed performances.

TABLE I
MAIN CHARACTERISTICS OF THE DESIGNED OP-AMP

	Conventional	Proposed
g_{m3}(μA/V)	910	910
g_{mf}(μA/V)	910	1940
$(w/l)_{10}$	61/0.6	130/0.6
$(w/l)_{11}$	18/0.6	11/0.6
SR^+/SR^- (V/μS)	3.5/4.2	4.1/4.2
t_{s+}/t_{s-}(ns)	340/164	151/168

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