International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:6, No:7, 2012

Electrical Characteristics of SCR - based ESD Device for I/O and Power Rail Clamp in 0.35um Process

Yong Seo Koo, Dong Su Kim, Byung Seok Lee, Won Suk Park, Bo Bea Song

***Abstract*—**This paper presents a SCR-based ESD protection devices for I/O clamp and power rail clamp, respectably. These devices have a low trigger voltage and high holding voltage characteristics than conventional SCR device. These devices are fabricated by using 0.35um BCD (Bipolar-CMOS-DMOS) processes. These devices were validated using a TLP system. From the experimental results, the device for I/O ESD clamp has a trigger voltage of 5.8V. Also, the device for power rail ESD clamp has a holding voltage of 7.7V.

***Keywords*—**ESD (Electro-Static Discharge), ESD protection device, SCR (Silicon Controlled Rectifier), Latch-up

I. Introduction

ELECTROSTATIC DISCHARGE(ESD) has been considered as a major reliability threat in the semiconductor industry. It was reported that ESD and EOS are responsible for up to 70% of failures in IC technology [1]. Therefore, each I/O PAD and power-rail (between VDD and VSS) must be designed with an ESD protection device that creates a discharge path for ESD current. The schematic of whole chip ESD clamp are shown in Fig. 1. As a process technology scales down, the design of ESD protection circuit becomes more challenging [2]. Also the effectiveness of ESD protection device is seriously degraded by advanced technologies, especially when a lightly doped drain (LDD) structure and salicide diffusion are used [3]. Silicon Controlled Rectifier (SCR) device, which can sustain a high ESD level within a small silicon area, is commonly used for ESD protection in advanced processes technology [4] –[6]. But, a SCR has a relatively high triggering voltage (about 20V) and its inherent positive feedback mechanism leads to strong snapback characteristics with a small holding voltage (about 1.7~2V) [7].The SCR device have a higher trigger voltage (about 20V), which is generally greater than the gate-oxide breakdown voltage of the input stage. Therefore, the SCR devices need to reduce trigger voltage lower then gate oxide breakdown voltage of the input stage.

Yong Seo Koo is with the Department of Electronics and Electrical Engineering, Dankook University, Gyeonggi-do, S. Korea, (e-mail: yskoo@dankook.ac.kr).
Dong Su Kim is with the Department of Electronics and Electrical Engineering, Dankook University, Gyeonggi-do, S. Korea, (e-mail: pojangzi@dankook.ac.kr).
Byung Seok Lee is with the Department of Electronics and Electrical Engineering, Dankook University, Gyeonggi-do, S. Korea, (e-mail: bangbang01@dankook.ac.kr).
Won Suk Park is with the Department of Electronics and Electrical Engineering, Dankook University, Gyeonggi-do, S. Korea, (e-mail: nwo413@dankook.ac.kr).
Bo Bea Song is with the Department of Electronics and Electrical Engineering, Dankook University, Gyeonggi-do, S. Korea, (e-mail: dkflgkak@nate.com @dankook.ac.kr).

Also, if the device is applied as a power clamp between the VDD and VSS, there is a possibility that the SCR could be triggered by unwanted noise and latch-up stimuli may also occur during normal operation. Therefore, it is difficult to design an SCR device for ESD power clamp. The latch-up issue can be overcome by increasing the holding voltage or current. This paper presents the SCR-based ESD protection devices that provide a low trigger voltage and high holding voltage for I/O ESD clamp and power-rail ESD clamp, respectably. Also, these devices are fabricated by using 0.35 um BCD processes.

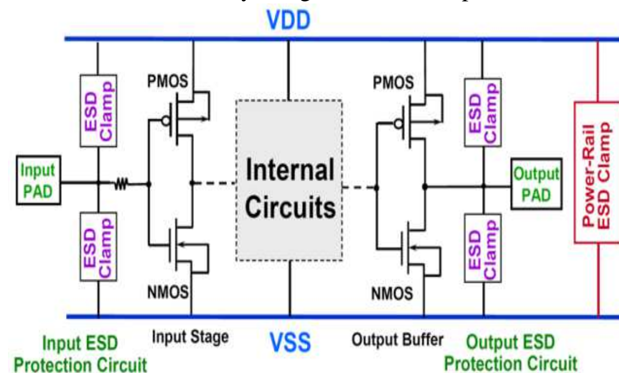

Fig. 1 The schematic of whole chip ESD clamp

II. Device description

A. The device for power rail clamp

Fig. 2 shows a cross-sectional view of the ESD protection device for power rail ESD clamp. This device is made by adding a 2-finger-ggNMOS structure and p+ tab on the conventional SCR with an n+ bridge diffusion a cross the n/p-well junction. The 2-fingerggNMOS is formed on the right-hand side of the device to reduce trigger voltage and to generate the trigger current. The p+ tab is formed at the center of the conventional SCR and connected to the center diffusion (source of the ggNMOS) of ggNMOS. The p+ tab provides the p-well on the left-hand side of the device with the self-trigger current generated by ggNMOS. A parasitic diode is imbedded in the structure. In negative stress mode, the device operates as a diode to discharge ESD current. Under normal operating conditions, the ESD protection device is in the off state, thus this device is not operating as an ESD protection device. But when the PAD voltage increases (As ESD occur to PAD), the potential of n-well and drains of ggNMOS stack increase. Eventually, the drains of the ggNMOS stack and p-well junction begin to avalanche because the high electric field crosses it, then electron–hole pairs are generated.

International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:6, No:7, 2012

The holes drift towards p-substrate contact and strengthen a potential of p-well, and the potential from the center diffusion of the ggNMOS stack to the substrate junction increases and gives forward biases at this junction. Two parasitic npn bipolar transistors turn-on and the current 'Path1' is formed as shown in Fig. 2. This trigger current flows towards p+ cathode through p+ tab/p-well. As trigger current increases, p-well/n+ cathode junction forward biases. The parasitic npn bipolar (collector: n+/n-well anode, base: p-well, emitter: n+ cathode) and the parasitic pnp bipolar (collector: p+ anode, base: n-well, emitter: p+ cathode) turn on. Then, the current which is mostly discharged is passed through 'Path2' as shown in Fig 2. On the other hand, when a negative bias is applied on the pad with a grounded line, the parasitic diode (p+ cathode/p-well or p-substrate/n-well/n+ anode) in the ESD device will be forward biased to discharge the negative ESD current.

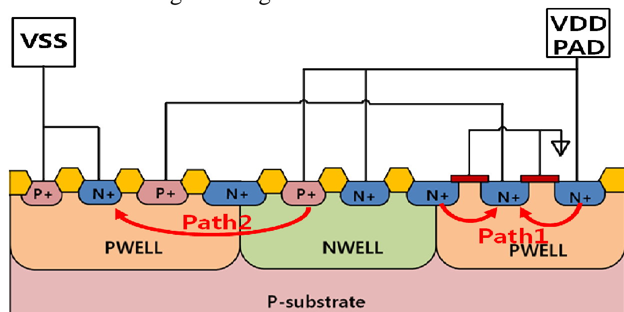

Fig. 2 The cross-sectional view of the power rail ESD device

B. I/O ESD clamp device

Fig. 3 shows a cross-sectional view of the ESD protection device for I/O ESD clamp. This device is made by adding the low voltage trigger SCR (LVTSCR) structure and p+ trigger node on the conventional SCR with a n+ bridge diffusion across the n/p-well junction. The LVTSCR is formed on the right-hand side of the device to reduce trigger voltage and to generate the trigger current. The p+ tab is formed at the center of the conventional SCR and connected to the cathode of LVTSCR. The p+ tab provides the p-well on the left-hand side of the device with the self-trigger current generated by LVTSCR. Also, the n+ tab on the left-hand side of the conventional SCR provides the trigger current to the right-hand side of p-well diffusion area. Under normal operating conditions, the LVTSCR is in the off state and thus the main SCR is not operating as an ESD protection device. This is because the breakdown voltage of the main SCR is higher than the supply voltage. Therefore, the ESD protection device does not have an effect on the internal core circuit. When positive ESD surge is applied to the I/O PAD, on the other hand, the LVTSCR of low trigger voltage compared to the main SCR, has an avalanche breakdown and the LVTSCR is turned on. And then, the generated current by avalanche breakdown is injected to the left-hand side of p-well on main SCR. As a result of this trigger current injection, the potential barrier is lower and thus the trigger voltage of main SCR decreases. On the other hand, when a negative bias is applied on the I/O PAD with a grounded line, the parasitic diode (p+ cathode/p-well or p-substrate/n-well/n+ anode) in the ESD device will be forward biased to discharge the negative ESD current.

TABLE I
AN EXPERIMENTAL RESULT COMPARATIVE

	Trigger Voltage (V)	Holding Voltage (V)	Second breakdown current (A)	HBM (kV)	MM (V)
I/O ESD clamp device	5.8	3	6.3	8	600
Power rail ESD clamp device	8.5	7.7	4.1	7.5	450

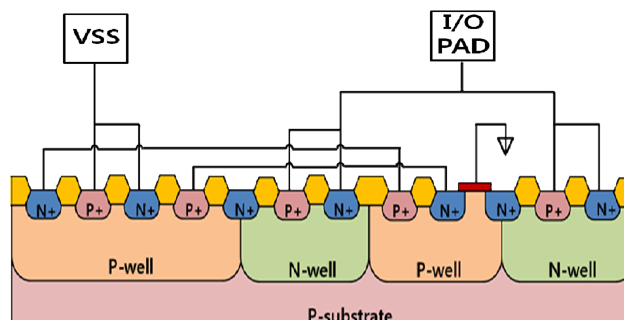

Fig. 3 The cross-sectional view of the I/O ESD clamp device

III. EXPERIMENTAL RESULTS

A. TLP(Transmission Line Pulse) system

The TLP is typically presented as a plot of the current versus the voltage showing a parameter, such as the turn-on point (Vt1, It1) of the snapback protection structure. Other parameters, such as the on-resistance can also be easily found in the TLP I-V curve. A rectangular pulse can be obtained when discharging an open-ended transmission line width 50 ohm impedance over an attenuator as shown in Fig. 4 (a). The transmission line is charged via a high voltage power supply and discharged via a switch. The current and voltage values are captured after the attenuator. A short coaxial cable connects the attenuator with the device under test (DUT). The I-V characteristic and DC-leakage current has been measured with a transmission line pulse (TLP) tester with a pulse duration of 100ns, rising time of 10ns. Fig. 4 (b) shows the TLP voltage pulse of the conventional

B. TLP I-V characteristics (Power rail ESD clamp device)

The pulsed IV-characteristics and the DC leakage current evolution of the ESD protection device for power rail ESD clamp device is shown in Fig. 5. This SCR-based device has a width of 50um.

In Fig. 5, TLP-measured the trigger voltage (Vt), holding voltage (Vh) and second breakdown current (It2) of the power rail ESD clamp device is 8.5V, 7.7V and 4.1A, respectively.

The power rail ESD clamp device has higher holding voltage (about 7.7V) than conventional SCR (about 1.7V~2V). This electrical characteristics help to avoid latch-up problem. As a result this device can provide improved performance for power rail ESD clamp

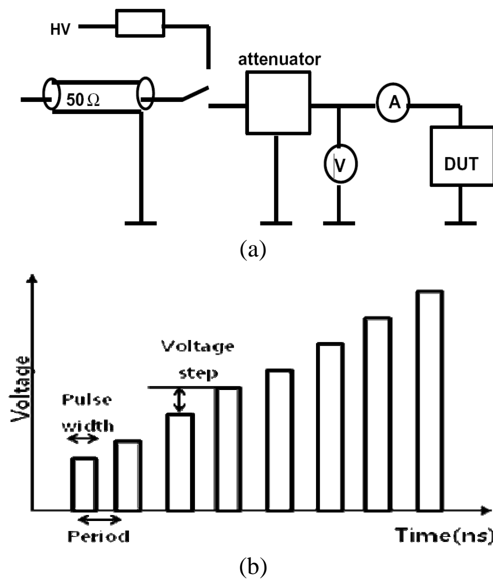

Fig. 4 (a)The equivalent circuit and (b) voltage pulse of TLP model

C. TLP I-V characteristics (I/O ESD clamp device)

The pulsed IV-characteristics and the DC leakage current evolution of the ESD protection device for I/O ESD clamp device is shown in Fig. 6. This device has a width of 60um.

In Fig. 6, TLP-measured the trigger voltage (Vt), holding voltage (Vh) and second breakdown current (It2) of the I/O ESD clamp device is 5.8V, 3V and 6.3A, respectively. This device has lower trigger voltage (about 5.7V) than conventional SCR (about 20V). As a result this device can provide improved performance for 1.8V and 3.3V I/O ESD clamp.

D. ESD Robustness (HBM/MM test)

The results from the TLP test with the 100ns pulse width can be well correlated to the HBM (Human Body Model). This has been well established in recent reports [8], [9]. However, a miscorrelation between the TLP and the HBM still exists because of the system's limitation and its testing environments [10], [11]. Fig. 6 shows the standard model for a HBM/MM ESD event.

The HBM (Human Body Model) and MM (Machine Model) ESD robustness of the proposed devices are measured by the ESS-6008 ESD simulator. The failure criterion is defined as a 20% current shift from the original I-V curve at operating voltage+10%.

The ESD protection device for power rail ESD clamp passes an ESD test of HBM 7.5kV and MM 450 V. And the device for I/O ESD clamp passes an ESD test of HBM 8kV and MM 600V. All the devices meet commercial standards (HBM 2kV, MM 200V).

Table I is present to an experimental result comparative of I/O and power rail ESD clamp devices.

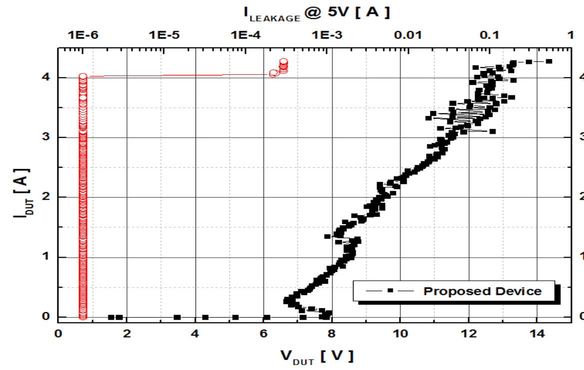

Fig. 5 TLP I-V characteristics of power rail ESD clamp device

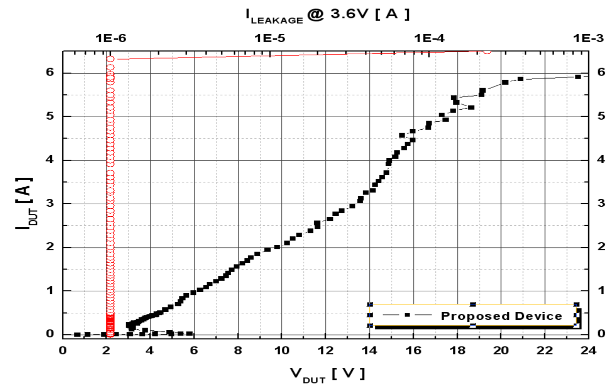

Fig. 6 TLP I-V characteristics of I/O ESD clamp device

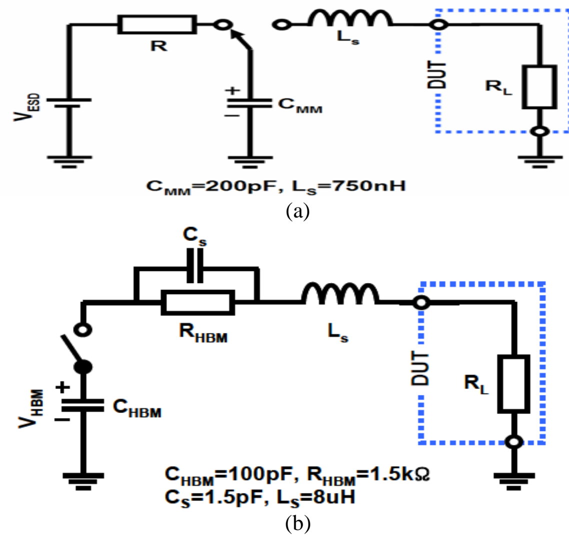

Fig. 7 Standard model for (a) HBM and (b) MM

IV. Conclusion

This paper presents a SCR-based ESD protection device for I/O and power rail clamp, respectability. These ESD protection devices have a lower trigger voltage and high holding voltage than conventional SCR. The ESD protection devices are fabricated by using 0.35um BCD process. From the experimental results, The SCR- based ESD device for I/O ESD clamp has a trigger voltage 5.8V and holding voltage3V, is for

1.8V and 3.3V I/O applications. Also, the device for power rail ESD clamp has a trigger voltage 8.5V and holding voltage7.7V. This device with latch-up immune characteristic can provide improved performance for power rail ESD clamp.

ACKNOWLEDGMENT

This research was supported by the Ministry of Knowledge Economy, Korea, under the University ITRC support program supervised by the National IT Industry Promotion Agency (NIPA-2012-C1090-1201-0003) and Industrial Strategic Technology Development Program funded by the Ministry of Knowledge Economy (10039145, The development of system semiconductor technology for IT fusion revolution)

REFERENCES

[1] Huang, et al.., "ESD protection design for advanced CMOS," in *Proc. SPIE,* 2001, pp. 123–131.

[2] R.G Wagner, J. Soden and C.F. Hawkins, "Extend and cost of EOS/ESD Damage in an IC Manufacturing Process," in *Proc. of the 15th EOS/ESD Symp.*,2005, 1993, pp. 49–55.

[3] M.D. Ker and C.H. Chuang, "ESD Implantations in 0.18um Salicided CMOS Technology for On-Chip ESD Protection with Layout Consideration", *Int. Symp. Physical and Failure Analysis of Integrated Circuits*, 2001, pp. 85-90.

[4] C. Russ, M. Mergens, J. Armer, P. Jozwiak, G. Kolluri, L. Avery, and K.Verhaege, "GGSCRs: GGNMOS triggered silicon controlled rectifiers for ESD protection in deep submicron CMOS processes," in *Proc*. EOS/ESD Symp., 2001, pp. 22-31.

[5] M.-D. Ker and K.-C. Hsu, "Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits," *IEEE Tran. Device Mater. Reliab*. vol. 5, no. 2, Jun 2005, pp. 235–249.

[6] P.-Y. Tan, M. Indrajit, P.-H. Li, and S. H. Voldman, " RC-triggered PNP and NPN simultaneously switched silicon controlled rectifier ESD networks for sub-0.18μm technology," in *Proc. of IEEE Int. Symp. On Physical and Failure Analysis of Integrated Circuits*,2005, pp. 71–75.

[7] V. Vashchenko, A. Concannon, M. ter Beek, and P. Hopper, "High holding voltage cascaded LVTSCR structures for 5.5-V tolerant ESD protection clamps," *IEEE Trans. Devices Mater. Rel.*, vol. 4, 2004, pp. 273–280.

[8] O. Semenov, et al, "ESD Protection Device and Circuit Design for Advanced CMOS Technologies," *Springer*. 2008.

[9] J. Barth, Koen Verhaege, Leo G. Henry, and J. Richner, "TLP Calibration, Correlation, Standards, and New Techniques," *Proc. EOS/ESD Symp*., 2000, pp. 85-96.

[10] W. Stadler, X. Guggenmos, P. Egger, H. Gieser and C. Musshoff, "Does the TLP Failure Current obtained by Transmission Line Pulsing always correlate to Human body model tests," *Proc. EOS/ESD Symp*, 1997, pp. 336-372.

[11] G. Notermans, P. de Jong and F. Kuper, Pitfalls, "when correlating TLP, HBM and MM testing", *Proc. EOS/ESD Symp*, 1998, pp 170-176