

# 20 GHz Fractional Phased Locked Loop Circuit for the Gbps Wireless Communication

Ki-Jin Kim, Sanghoon Park, and K. H. Ahn

**Abstract**—This paper presents the 20-GHz fractional PLL (Phase Locked Loop) circuit for the next generation Wi-Fi by using 90 nm TSMC process. The newly suggested millimeter wave 16/17 pre-scaler is designed and verified by measurement to make the fractional PLL having a low quantization noise. The operational bandwidth of the 60 GHz system is 15 % of the carrier frequency which requires large value of  $K_v$  (VCO control gain) resulting in degradation of phase noise. To solve this problem, this paper adopts AFC (Automatic Frequency Controller) controlled 4-bit millimeter wave VCO with small value of  $K_v$ . Also constant  $K_v$  is implemented using 4-bit varactor bank. The measured operational bandwidth is 18.2 ~ 23.2 GHz which is 25 % of the carrier frequency. The phase noise of -58 and -96.2 dBc/Hz at 100 KHz and 1 MHz offset is measured respectively. The total power consumption of the PLL is only 30 mW.

**Keywords**—Millimeter Wave Fractional PLL, Wide band VCO, WPAN Transceiver.

## I. INTRODUCTION

THE 57-66 GHz band has been allocated for high data WPAN (Wireless Personal Area Network), wireless HD and next generation Gbps Wi-Fi. As defined by IEEE 802.15.3c and 802.11ad standards, four channels of 2.16 GHz bandwidth are allocated for 7 Gbps communication in 16 QAM (Quadrature Amplitude Modulation). However, it is still challenging work to realize 16-QAM communication in 60 GHz mainly due to performance of the PLL phase noise. The required phase noise for 16-QAM was reported in previous study [1]. It showed that the phase noise of below -90 dBc/Hz at 1 MHz offset is required for ignoring BER degradation from phase noise of the PLL.

Previously reported CMOS PLLs were mainly integer type synthesizers [2], [3] because it is difficult to realize the pre-scaler at the millimetre wave frequency. The integer PLL is limited in usage because the output frequency of the PLL is defined to integer multiple value of the TCXO (Temperature Compensated Crystal Oscillator). According to the ECMA standard, the channel bonding which combines two or four channels of 2.16 GHz band is introduced. Considering channel

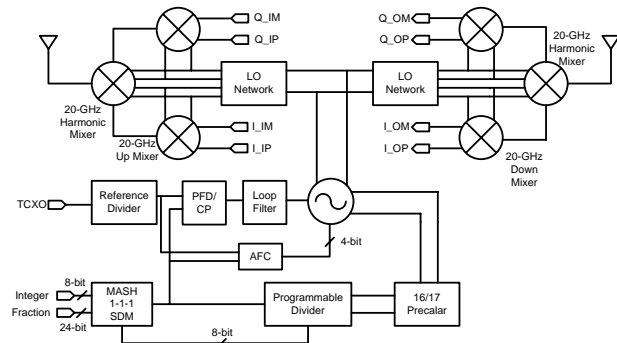


Fig. 1 Block diagram of the PLL and transceiver architecture

bonding requiring fractional frequency generation, a millimeter waver fractional PLL is imperative in future 60 GHz system.

This paper presents the 20-GHz fractional PLL with 4-bit controlled VCO. The reason why the 20 GHz is chosen for 60 GHz system is illustrated in the following section. To minimize fractional quantization noise, 20-GHz 16/17 pre-scaler is proposed. In section II, the suggested structures of VCO and pre-scaler are illustrated. In section III, the other circuits such as CP (Charge Pump), and PFD (Phase Frequency Detector) are illustrated. The measurement results are shown in section IV and the conclusions are drawn in section V.

## II. PROPOSED STRUCTURE OF THE VCO AND 16/17 PRE-SCALAR

As mentioned before, the requirement of the phase noise for the 60 GHz systems is lower than -90 dBc/Hz at 1 MHz offset frequency. The direct generation of the 60 GHz signal by CMOS VCO [2] showed a poor phase noise result mainly due to the passive losses from capacitors and varactors at 60 GHz frequency. The 60 GHz signal generated by push-push VCO [4] had harmonic and low output power problems. The injection locking oscillator [5] used two bulky additional LC tank oscillators that are susceptible to the process variation. It also took double the silicon die size comparing to other researches.

In order to resolve the phase noise issue, a 20 GHz only sliding IF architecture is proposed and illustrated in Fig. 1. Up/Down mixers are composed of 20 GHz mixers and 20 GHz sub-harmonic mixers. The 20 GHz sub-harmonic mixers translates 20 GHz input signal into 60 GHz output signal and vice versa. Therefore the VCO with the 20 GHz oscillation 20 GHz is the only local signal that is required for the 60 GHz system. By using one third of the system frequency, the design

Ki-Jin Kim is with the Korea Electronics Technology Institute, Gyeonggi-do, Korea (corresponding author to provide phone: 82-31-789-7226; fax: 82-31-789-7259; e-mail: sergeant@keti.re.kr).

Sanghoon Park and K. H. Ahn are with the Korea Electronics Technology Institute, Gyeonggi-do, Korea (corresponding author to provide phone: 82-31-789-7225; fax: 82-31-789-7259; e-mail: khajoh@keti.re.kr).



differential CP, the designed S-to-D block generates differential control signals and their symmetric wave forms are reinforced by the cross coupled inverters.

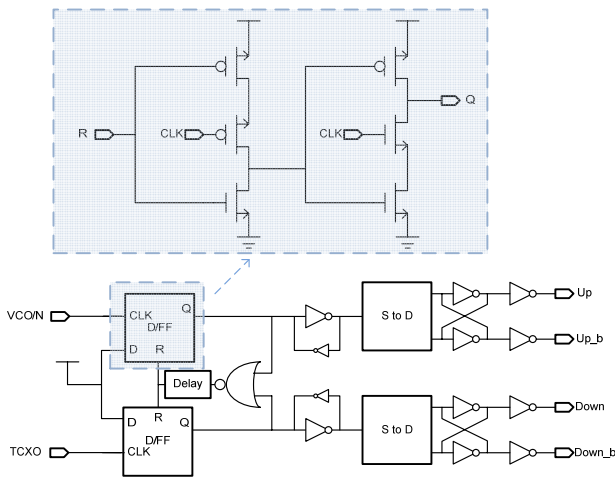


Fig. 4 Phase frequency detector with differential control output

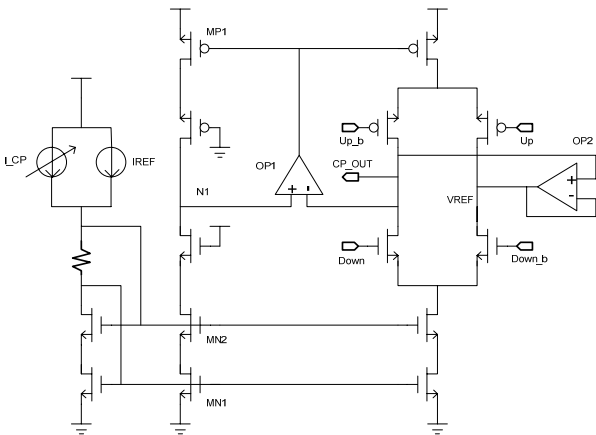


Fig. 5 Proposed charge pump circuit

The CP circuit is ideally parallel connection of current source and current sink which are implemented by PMOS and NMOS. However, the output resistance of the sub-micron transistor is not large enough to be modeled as a current source and sink. Therefore, a current mismatch occurs due to the difference between the drain-source voltages of the PMOS and NMOS when dumping the charge to the LF. A cascode structure boosts output resistance by the gain of the common source amplifier. However the cascode structure reduces voltage headroom and legroom of the CP output so the structure is not popular under the sub-micron technology. Another dominant problem in designing the low noise CP is charge sharing. When the CP switches are open, the drain voltage of PMOS is pre-charged to VDD and drain voltage of NMOS is discharged to GND due to the parasitic capacitance of the transistor. When the switches are closed, the output capacitor charges are shared with pre-charged or discharged

parasitic capacitor which causes voltage ripple at every switching cycle.

Fig. 5 illustrates the designed CP circuit. The current sink is implemented with the cascode structure (MN1 and MN2).

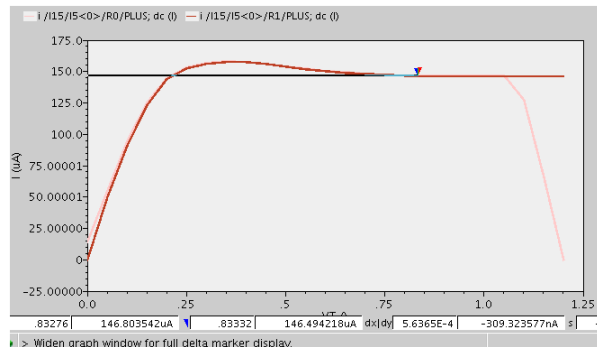


Fig. 6 Simulated DC characteristics of the proposed charge pump

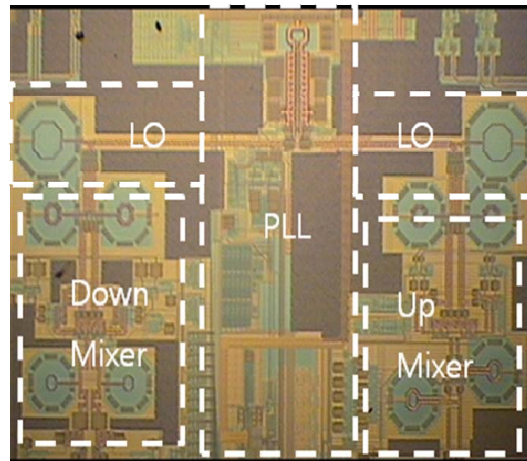


Fig. 7 Fabricated chip photo

The voltage legroom is secured by designing additional current source  $I_{CP}$  which is  $CP\_OUT$  (output voltage) dependent (inversely proportional) current source. As the  $CP\_OUT$  approaches to GND, more current is supplied to the CP then conduction current limitation caused by reduced legroom is compensated. The  $OP1$  adjust gate voltage of  $MP1$  with respect to the current of  $MN1$ . Also  $OP1$  makes the node  $N1$  the same with the  $CP\_OUT$ , therefore the reference current is exactly mirrored to the core of the CP regardless of  $CP\_OUT$ . In this way, current mismatch problem is minimized.

Differential architecture as shown in Fig. 5 guarantees constant current conduction to the CP core regardless of control signal. Constant current conduction mitigates charge sharing problems considerably, but the voltage difference between  $CP\_OUT$  and  $VREF$  still generates charge sharing. The inserted  $OP2$  is designed to eliminate above mentioned problem by making the two nodes equal. The simulation results show that the current mismatch is bounded within 300 nA with 0.2 ~ 1.1 V output operating range.

#### IV. MEASUREMENT RESULTS

The Fig. 7 is the die photograph of the fabricated design using TSMC 90 nm CMOS process. The reference frequency of the TCXO used in this paper is 50 MHz. The circuit draws the maximum 30 mW for PLL from a 1.2 V supply. The measured PLL frequencies, 18.2 ~ 23.2 GHz, which are translated into 54.6 ~ 69.4 GHz covers all 60-GHz band with enough margin.

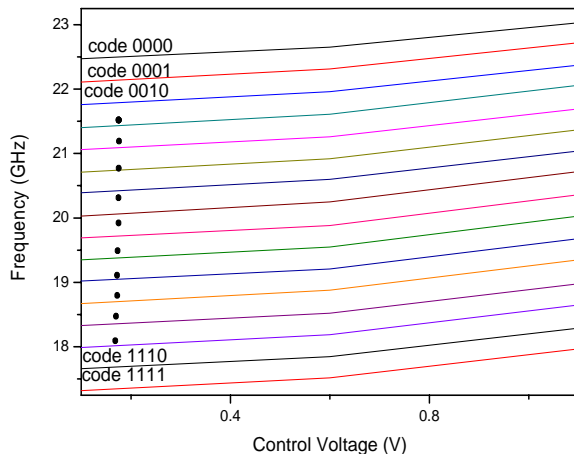


Fig. 8 Measured frequency characteristics of the PLL

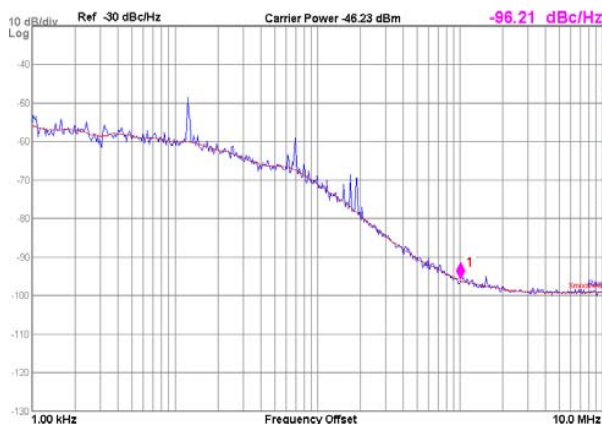


Fig. 9 Measured phase noise @ 20 GHz

The frequency range is measured by manipulating 8-bit integer programmable divider and 24-bit fractional SDM. Therefore the operation of the proposed pre-scaler is confirmed as far as 23.2 GHz. The measured tuning range is 25%. By using switchable fifteen capacitor arrays and four varactor arrays, the constant  $K_v$  is measured and well matched with simulation result (in Fig. 8). Due to the constant  $K_v$ , loop characteristics of all the resonance frequency is almost equal. The operational range of the CP is from 0.15 V to 1.09 V which is quiet well matched with simulation result. As a representative case, the phase noise of 20 GHz is selected and plotted in Fig. 9. A -58 dBc/Hz in-band noise and a -96.21 dBc/Hz noise at 1-MHz are measured. The measurement results shows that the proposed fraction PLL ensure 16 QAM data

communication in 60 GHz frequency.

#### V. CONCLUSION

A mm-wave fractional PLL frequency synthesizer was implemented in 90 nm CMOS process. The proposed VCO showed wide tuning range and constant  $K_v$  characteristics due to the combination of the capacitor and varactor arrays. The 20-GHz pre-scaler worked well as high as 23 GHz. The measured frequency and voltage tuning characteristics were well matched with simulation. The proposed circuit met the phase noise requirement of the 60 GHz system. Thus, the presented design can be a good PLL candidate for 60 GHz high speed wireless communication.

#### ACKNOWLEDGMENT

This work was funded by Ministry of Knowledge Economy and the project name is "Design of 60GHz Analog Beam Former". Fabrication was provided by TSMC. We thank Korea Advanced Institute of Science and Technology for their support in design and test.

#### REFERENCES

- [1] K. Okada, N. Li, K. Matsushita, K. Bunsen, R. Murakami, A. Musa, T. Sato, H. Asada, N. Takayama, S. Ito, W. Chaivipas, R. Minami, T. Yamaguchi, Y. Takeuchi, H. Yamagishi, M. Noda, and A. Matsuzawa, "A 60-GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver for IEEE 802.15.3c," *IEEE Journal of Solid State Circuits*, vol. 46, no. 12, pp 2988-3004, Dec 2011.
- [2] F. Barale, P. Sen, S. Sarkar, S. Pinel, and J. Laskar, "A 60GHz-Standard Compatible Programmable 50 GHz Phase-Locked Loop in 90 nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 7, pp.411-413, July 2010.
- [3] Ja-Yol Lee, S. H. Lee, H. Kim, and H. K. Yu, "A 28.5-32.5-GHz Fast Settling Multichannel PLL Synthesizer for 60-GHz WPAN Radio," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 5, pp.1234-1246, May 2008.
- [4] B. Catli and M. Hella, "A 60 GHz CMOS Combined mm-wave VCO/Divider with 10-GHz Tuning Range," *CICC*, 2009, pp 665-668.
- [5] C. Lee, L. C. Cho, J. H. Wu, and S. I. Liu, "A 50.8-53 GHz Clock Generator Using a Harmonic-Locked PD in 0.13 CMOS," *TCASII*, vol. 55, no. 5, pp. 404-408, May 2008.
- [6] H. Knapp, T. F. Meister, M. Wurzer, K. Aufinger, S. Boguth, and L. Treitinger, "A Low Power 20 GHz SiGe Dual-Modulus Prescaler," *IEEE MTT-S Digest*, pp 731-734, 2000.
- [7] M. A. Do, X. P. Yu, J. G. Ma, K. S. Yeo, R. Wu, and Q. Z. Zhang, "A 2GHz Programmable Counter with new re-loadable D Flip-flop," *IEEE EDSSC*, pp 269-272, 2003.