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Design and Simulation Interface Circuit for Piezoresistive Accelerometers with Offset Cancellation Ability

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***Abstract*—**This paper presents a new method for read out of the piezoresistive accelerometer sensors. The circuit works based on Instrumentation amplifier and it is useful for reducing offset In Wheatstone Bridge. The obtained gain is 645 with 1μv/°c Equivalent drift and 1.58mw power consumption. A Schmitt trigger and multiplexer circuit control output node. a high speed counter is designed in this work .the proposed circuit is designed and simulated In 0.18μm CMOS technology with 1.8v power supply.

***Keywords*—**Piezoresistive accelerometer, zero offset, Schmitt trigger, bidirectional reversible counter.

I. Introduction

THE Piezoresistive accelerometers consist large families of MEMS accelerometer and their applications in intelligent systems are increasing day by day. Therefore designing an appropriate interface circuit for read out of the sensor that is low noisibility and power consumption with high resolution is very important. The piezoresistive accelerometers also have numerous applications in medical industries, for example a micro power integrator circuit is required to measure accelerations of the human body motion. This circuit is intended to be employed in the construction of rate-adaptive cardiac pacemakers (a pacemaker which varies its stimulation rate according to patient's requirement) [1]. Another application is based on fuel control system for automobiles that primarily to be used in Engine Control Unit (ECU) [2]. Zero-offset would occur when the Wheatstone bridge of the Micro-accelerometer does not match. The Common-mode level of output signal would exceed the circuits' -operating voltage range when the gain of interface circuit is relatively large. This would lead to the failure of differential input signals detection, thus the micro-accelerometer works abnormally [3]. In this work we fulfill one suitable circuit to meet the above objectives and in the following we will review the details.

II. Main Operation of the Circuit

In this part we propose and study about a suitable circuit for reading of the sensor. The circuit is basically consisted of one instrumentation amplifier an accumulator, a comparator, a bidirectional reversible counter, a latch and a digital to analog converter circuit. On the side, this circuit also must have a Schmitt trigger and multiplexer that will be explained later. The schematic diagram of proposed circuit is shown in Fig. 1.

The circuit will work in 2 states, first we suppose the bridge is in stasis. In this state offset voltage must be removed and we did it by differential op-amp, Schmitt trigger and multiplexer. Circuit operation is as follows:

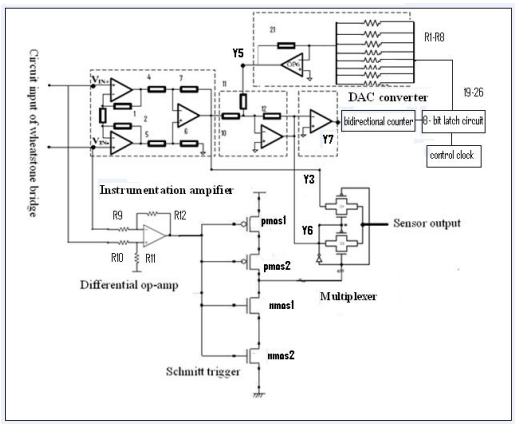

Fig. 1 Schematic diagram of the proposed circuit

When the bridge output is in offset scope, the differential op-amp will amplify it and send to Schmitt trigger. The Schmitt trigger circuit is designed so that its output in offset range is high and transfer the y6 output to sensor output by multiplexer. And when there is a major acceleration, the Schmitt trigger output will be low and instrumentation amplifier output (y3) will transfer to sensor output by multiplexer.

The main operation of digital feedback loop is as follows: when the offset voltage is coming, by instrumentation amplifier will amplify and send to accumulator. In this part amplified signal and counter digital output are subtracted and send to comparator. If the accumulator output is zero, the comparator output will be high impedance and counter does not work. If there is a difference, the counter circuit will count up or down, depending on the comparator output, for reducing the offset voltage. The latch circuit is designed for locking the counter output in the DAC input. The DAC circuit will convert the counter digital output to analog signal and V_{ref} is 0.9 volt with 3 mv adjustment precision and 0 to 896mv correction voltage scope.

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III. Operational Amplifier Circuit

The OP-AMP circuit that we used in instrumentation amplifier is shown in Fig. 2.

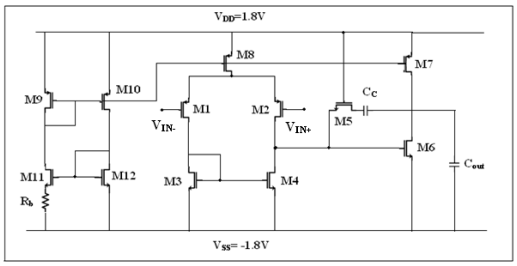

Fig. 2 Operational amplifier circuit

CMOS technology is favored here, because characteristics and performance of the devices can be designed by changing the sizes (length and width) of the MOSFETs used [2]. Also BiCMOS technology is avoided to reduce fabrication process complexity. The TSMC 0.18um technology is used due to its high transconductance, high output impedance and low threshold voltage as well as small chip area of the device [4].

The testing results of this circuit are as follows:

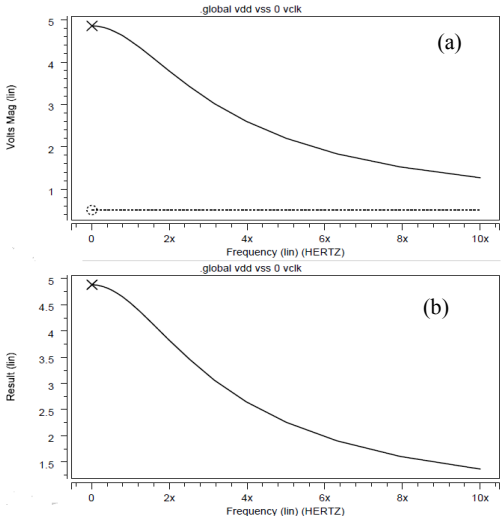

Fig. 3 Output voltage (a) and bode diagram(b) of OP-AMP up to 10MHz frequency

Fig. 3 shows the open loop gain equal to 10 that in frequencies near to 5 MHz will reduce. The power consumption of OP-AMP is attained equal to 152.16 µw.

IV. Instrumentation Amplifier Circuit

The instrumentation amplifier that we designed in this work is consisted of three OP-AMP that we designed and simulated it in last section. The main function of this circuit is to amplify weak signals read from the Wheatstone bridge. This part also transfer all offset signals to digital feedback loop for correction the entry offset voltages. The gain and power consumption of this circuit is shown in below (Fig. 4):

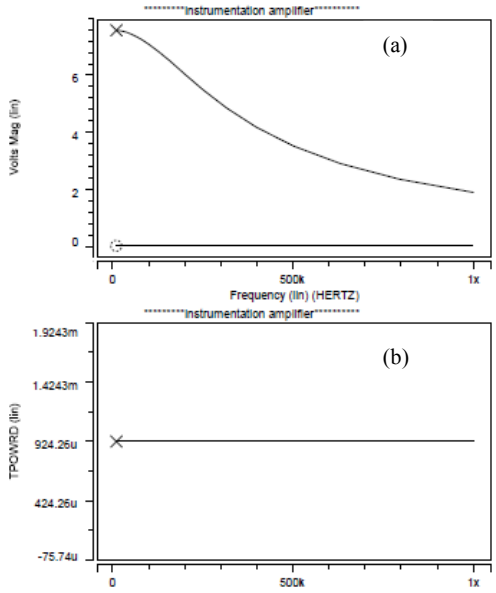

Fig. 4 Gain(a) and power consumption(b) of instrumentation amplifier

The first diagram is related to gain so that entry signal is about 10 mv and output about 6.45 Volt that show the circuit gain is about 645.in the second part of this graph we simulated the circuit power consumption equal to 924.26µw.

V. Comparator Circuit

The comparator circuit that we used in Fig. 1 is shown in Fig. 5.

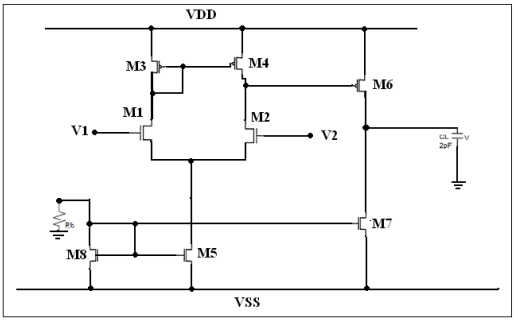

Fig. 5 Comparator circuit

The testing result of the comparator gives us the 20µw to 48µw power consumption and its output graph versus the input is shown in Fig. 6.

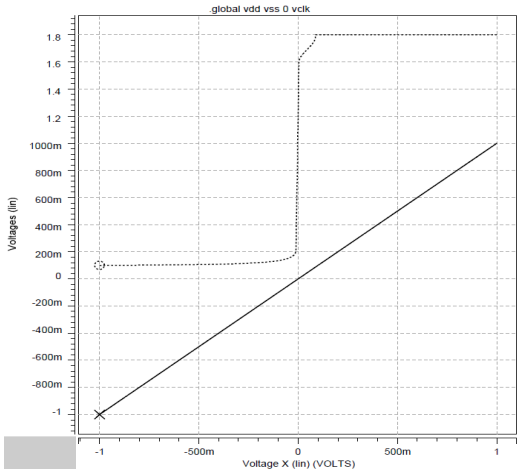

Fig. 6 Comparator output versus its input

VI. Up-Down Counter Circuit

For counter designation we use the jk-flip flop. The basic operation of the counter is as follow:

After the circuit starts, eight-digit bidirectional reversible counter is at the original state, with an output of "**00000000"**. This output is sent to the D/A switch after the latch. The reference voltage of D/A switch Vref is 0.9V. The output voltages of the instrumentation amplifier and the D/A switch make the subtraction. The obtained value is compared with the center voltage of the circuit. If the former is greater than the latter, the output of the comparator is 1, and the bidirectional counter is in the subtraction pattern, giving an output of 11111110; if the former is smaller than the latter, the output of the comparator is 0, and the bidirectional counter is in the addition pattern, giving an output of 00000001; The digital output of the counter is sent to the D/A switch after the latch. If the output voltage of the accumulator is higher than center voltage, the counter reduces once again, (output = 11111101); otherwise it outputs 00000010. By repeating this approach again and again, the goal of eliminating zero drift is gradually achieved. The counter block diagram and output simulation result is shown in Figs. 7 and 8 respectively [5].

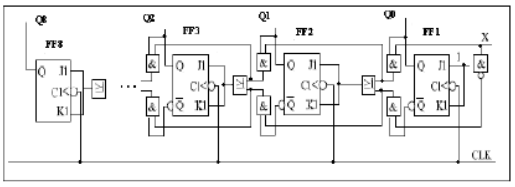

Fig. 7 Block diagram of up-down counter

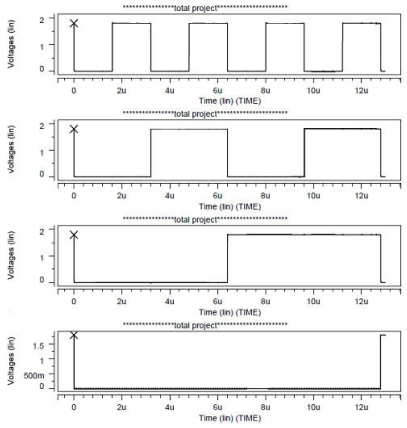

Fig. 8 Counter output diagram

The counter output shows that speed of designed circuit for counter is very suitable, because in 12 microseconds a complete cycle counter counts. It is very good result compared with last work in [5].

VII. Digital to Analog Converter Circuit

After each step that counting is completed the latch circuit must lock data on input of the DAC and DAC circuit must convert counter output to a proportional signal. The DAC circuit that we used is shown in Fig. 9.

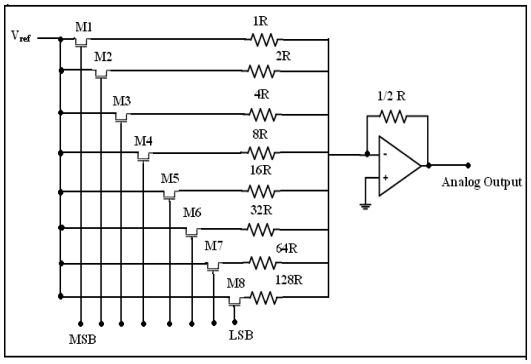

Fig. 9 Digital to analog converter circuit [6]

For calculating the resolution and correction voltage scope in designed DAC with V_{ref} = 0.9v we have:

If 0000 0000 (on DAC input) → V_{out}= 0

IF 1111 1111(on DAC input) →V_{out}=896mv

FROM 0000 0000 TO 0000 0001 (Changed voltage) = 3 mv

VIII. Schmitt Trigger Circuit

We designed the Schmitt trigger [7] circuit in this work so that for offset voltage(less than 700 mv) is low and for more than 700 mv is high. The Hspice output for this circuit is shown in Fig. 10.

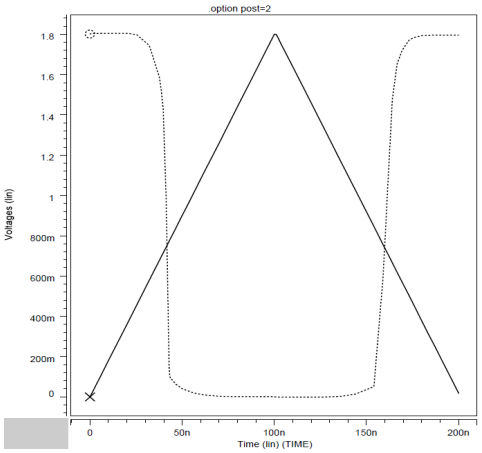

Fig. 10 Schmitt trigger simulation

IX. Simulation Result and Overall Circuit Optimization

After separate simulation for different part of the circuit we must optimize and simulate overall circuit. Figs. 11 and 12 show the diagram for removing the zero offset in transient and steady state, respectively.

In Figs. 11 and 12 the up diagram is input offset and down is circuit output at y3 node.

The noise that we have calculated for this circuit is electrical noise and it is calculated with attributing all noise sources to circuit entry and exit. In this state we assume that all of the internal elements are ideal. Simulation result presents a suitable electrical noise in entry equal to 71nv/√Hz.

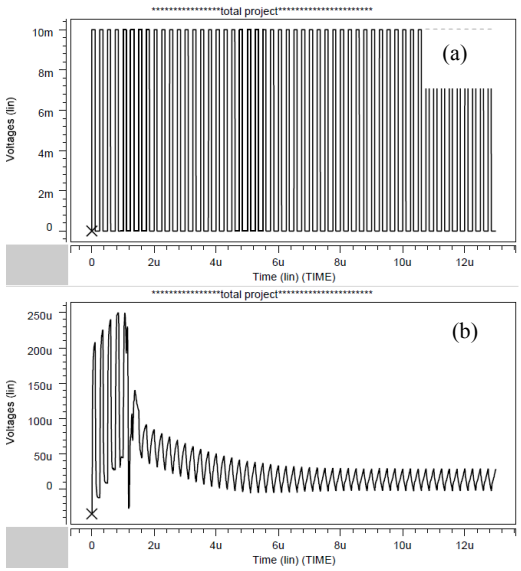

Fig. 11 Offset cancellation in transient state; input offset (a), output offset (b)

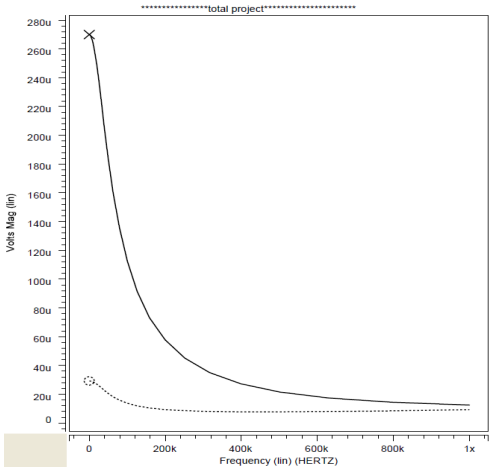

Fig. 12 Offset cancellation in steady state

Also for estimating the equivalent drift in circuit output, we simulated the output voltage at y6 node for the temperature range of -20°c to +60°c.this designation offer the maximum equivalent drift equal to 1µv/°c that is shown in Fig. 13.

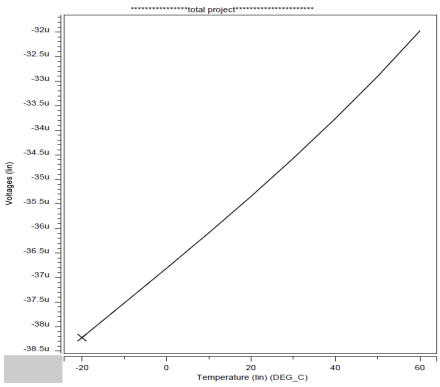

Fig. 13 Equivalent drift diagram in output node(y6)

X. Conclusion

This paper present an interface circuit for piezoresistive accelerometer that calibrate zero offset and has suitable specification included low noise-taking and power consumption compared with previous works. The circuit is designed and simulated in 0.18µm CMOS technology. All simulations have been carried out up to 10MHz frequency. In Table I we summarized the most important results.

TABLE I
Optimized Result in Designed Circuit

Supply voltage	**1.8v**
Gain	645
Input Offset Voltage Drifts Equivalent	1 µV/°C
Input Noise	71 nv/√Hz
Power Consumption	1.58 mw
Adjustment Precision	3 mw
Correction Voltage Scope	0−896 mv

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