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A Sub-mW Low Noise Amplifier for Wireless Sensor Networks

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Abstract—A 1.2 V, 0.61 mA bias current, low noise amplifier (LNA) suitable for low-power applications in the 2.4 GHz band is presented. Circuit has been implemented, laid out and simulated using a UMC 130 nm RF-CMOS process. The amplifier provides a 13.3 dB power gain a noise figure NF$<$ 2.28 dB and a 1-dB compression point of -15.69 dBm, while dissipating 0.74 mW. Such performance make this design suitable for wireless sensor networks applications such as ZigBee.

Keywords—Current Reuse, IEEE 802.15.4 (ZigBee), Low Noise Amplifiers, Wireless Sensor Networks.

I. Introduction

CMOS integrated circuits for RF applications are being intensely studied due to their potential for low cost, high scalability and integration that make them suitable for Systems on Chip (SoC) implementation [1]. The improvements experienced by RF-CMOS technology in the last years has disclosed several possible applications for wireless systems. Due to their flexibility and broad range of potential applications, wireless sensor networks operating in the unlicensed ISM band are the object of intensive research [2], [3], [4] and have been lately standarized by the IEEE [5]. The mobile nature and the low cost of such infrastructureless networks makes power consumption of paramount importance.

In this work a design based on current reuse [6] is presented. Current reuse is an effective technique to minimise power consumption since both the amplifier stages share the same bias current. Despite the low bias current, our design achieves excellent power gain and linearity in the operation band.

The rest of the paper is structured as follows: Section II describes the proposed low noise amplifier and addresses the design of the input and output matching networks, Section III issues the design trade-offs and reports the simulated performance. Finally, the conclusions are given in Section IV.

II. Proposed LNA

Fig. 1 shows the proposed LNA. Transistor M1 and M2 implement two cascaded common-source stages; however, transistor M2 is stacked on top of M1 in order to share the same bias current and the same RF grounds [6]. Input and output stages are matched to a 50 Ω source and load resistance respectively. Both transistors are minimum length and have the same channel width $W = 95$ μm. The size has been chosen in order to guarantee an acceptable stage gain at a low bias voltage.

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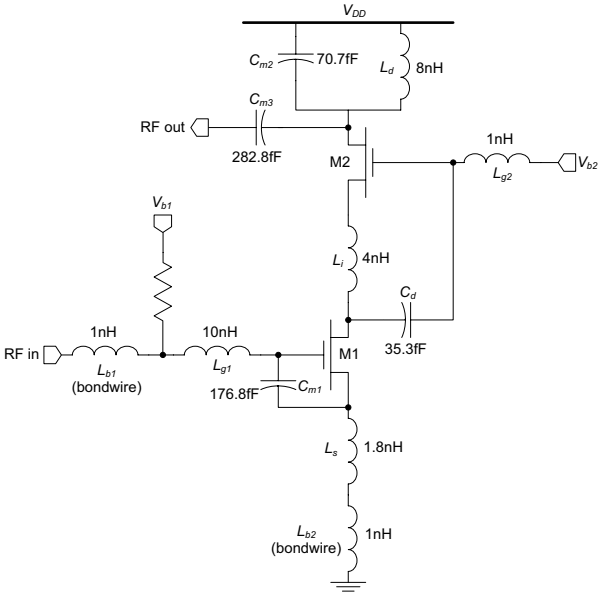

Fig. 1. The Proposed Current-Reuse LNA.

Bias voltages V_{b1} and V_{b2} are approximately 0.4 and 0.8 V respectively and have been chosen in order: (1) to guarantee that M1 and M2 are in deep saturation regardless of bias and supply voltage fluctuations, (2) to achieve a transconductance g_m sufficiently high to keep transition frequency ω_T high in order not to increase excessively the noise figure NF, and (3) to be easily generated with a simple on-chip active voltage divider.

Inductor L_i sizing is crucial in the design. In fact, this inductor affects input matching (through the Miller capacitance of transistor M1), inter-stage matching (with capacitance C_d) and input stage gain. In addition, this inductor also provides a DC path for biasing transistor M1, whereas performing stage decoupling at RF.

The stages biasing points are decoupled by capacitor C_d that acts like a DC blocker, whereas inductor L_{g2} provides a DC path for transistor M2 biasing and RF isolation to the bias network.

A. Matching

Input matching network is implemented by the the inductor $L_1 = L_{b1} + L_{g1}$, by source degeneration inductor $L_2 = L_{b2} + L_s$, and by the equivalent capacitor $C = C_{m1} + C_{gs1}$ formed by the matching capacitor C_{m1} and the gate-to-source capacitance C_{gs1} of transistor M1.

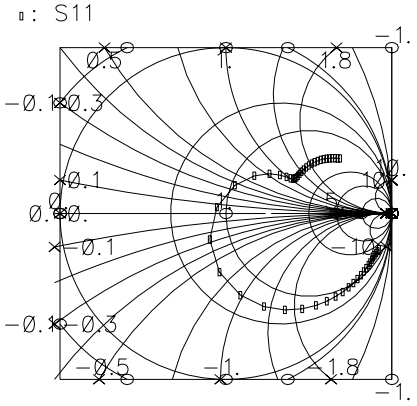

Fig. 2. Smith's Chart Diagram of LNA Input Matching Network.

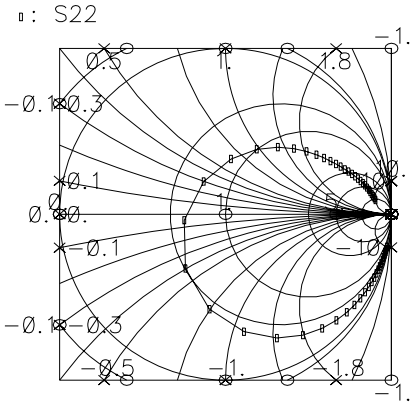

Fig. 3. Smith's Chart Diagram of LNA Output Matching Network.

The amplifier input impeadence $Z_i(\omega)$ is [7]:

$$Z_i(\omega) = g_{m1}\frac{L_2}{C} + j\left[\omega(L_1+L_2) - \frac{1}{\omega C}\right]. \qquad (1)$$

At the resonant frequency $\omega_0 = \frac{1}{\sqrt{(L_1+L_2)C}}$ the imaginary part of $Z_i(\omega)$ is cancelled and the real part is matched to the source impeadence $R_S = 50\ \Omega$ by carefully sizing transistor M1 transconductance g_{m1} and the passives L_2 and C. Equation (1) is used as a starting point to size the input matching network, since, as stated previously in this work, inductor L_i affects the stage input impeadence and may lead to instability if not adequately dimensioned. Fig. 2 shows the frequency behaviour of the input matching network. Best input matching is achieved at a frequency of 2.430GHz.

Output matching is performed by the capacitive divider formed by the capacitors C_{m2} and C_{m3}. Capacitor C_{m2} also resonates with inductor L_d improving both gain and narrow-band behaviour. Fig. 3 depicts the frequency behaviour of the output matching network Best output matching is achieved at a frequency of 2.449 GHz. Finally, Fig. 4 plots input and output scattering paramenters (s_{11} and s_{22}) in rectangular coordinates. Observe that in the band of interest $s_{22} < -10$ dB and $s_{11} < -21$ dB.

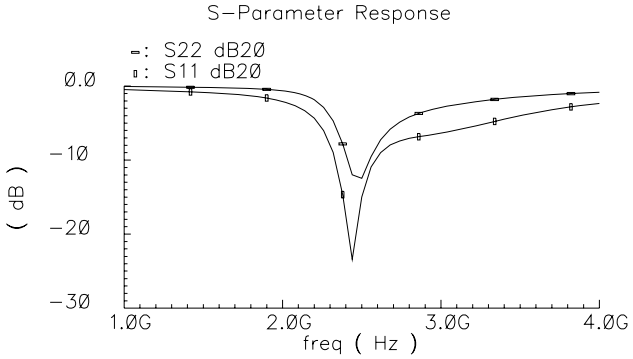

Fig. 4. LNA Input and Output Scattering Parameters.

III. Discussion

RF amplifiers design is a challenging task since the designer must meet a number of specifications such as gain, frequency response, noise figure, linearity, power consumption, input and output impedance. Most of these design parameters are competing (for example linearity and power consumption), this in turn requires finding compromises and trade-offs while tuning the design.

A. Gain

If Miller's effect on transistor M1 is neglected, the unity current gain frequency ω_T is given by:

$$\omega_T = \frac{g_{m1}}{C} \qquad (2)$$

so that at the resonant frequency $\omega = \omega_0$ the input impeadence becomes:

$$Z_i(\omega_0) = g_{m1}\frac{L_2}{C} = \omega_T L_2. \qquad (3)$$

The stage gain is determined by the stage transconductance $G_m = \frac{I_{ds1}}{V_{in}}$:

$$G_m \approx \frac{\omega_T}{j\omega_0(R_s + Z_i(\omega_0))} \approx \frac{\omega_T}{j\omega_0 2R_s} \qquad (4)$$

since at the resonant frequency source and amplifier must be matched in order to guarantee maximum power delivery to the load.

In order to increase G_m and maximise the stage gain, transistors must have a high transconductance. On the other hand, a high transconductance requires high bias currents and transistors overdrive voltages. Since low-power consumption is the main design constraint, gain must be traded-off for power. Transistors M1 and M2 have been designed in order to have approximately the same transconductance $g_{m1} \approx g_{m2} \approx 12.1$ mS and bias conditions $v_{gs1} \approx v_{gs2} \approx 370$ mV. Under these conditions, the transistors deliver a bias current of approximately 0.61 mA. In order to keep ω_T as high as possible, M1 and M2 have been sized to reduce the gate capacitance and hence C. With a channel width $W = 95\ \mu$m and a minimum length, the gate capacitance C_{gs1} is approximately 61.2 fF which, in turn leads to $C = C_{gs1} + C_{m1} = 238$ fF. Consequentely the unity current gain frequency is $\omega_T = 50.8$ Grad/s, that is a value big enough to guarantee a high

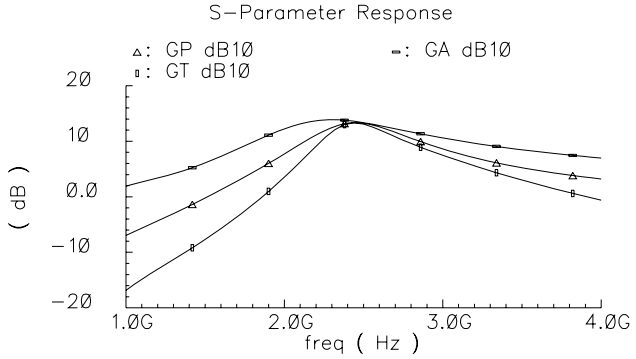

Fig. 5. The LNA Gain.

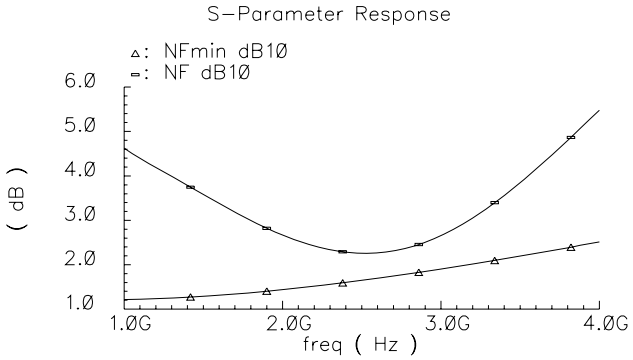

Fig. 6. The LNA Noise Figure.

stage transconductance G_m while mantaining low noise and low power consumption.

Fig. 5 depicts the tranducer power gain (G_T), the operating power gain (G_P), and the avalaible power gain (G_A) of our design. G_T is defined as the ratio of the power delivered to the load and the power available from the source; G_P is defined as the ratio between the power delivered to the load and the power input to the LNA; finally, G_A is defined as the power available from the LNA and the power available from the source. Since the power available from the source is greater than the power input to the LNA, $G_P > G_T$. The closer the two gains are, the better is the input matching. Similarly, since the power available from the LNA is greater than the power delivered to the load, $G_A > G_T$. The closer the two gains are, the better is the output matching. Fig. 5 shows a transducer power gain of 13.3 dB approximately in the band of interest.

B. Noise figure

According to [8] a conservative estimation of the noise figure (NF) of an inductive degenerated LNA implemented using a deep submicron process, may be carried out using equation (5):

$$NF = 1 + 5.6\frac{\omega_0}{\omega_T} \tag{5}$$

So, in order to improve noise figure, the unity current gain frequency ω_T must be as high as possible. Equation (5) predicts a noise figure $NF < 2.66$ dB for our design in the 2.4 GHz band. Fig. 6 represents the plots of both the noise figure and the minimum noise figure achievable. The simulated noise figure is $NF < 2.28$ dB in the band of interest and is close to the minimum achievable noise figure.

Finally Table I summarises the main noise contributions at 2.44GHz when the input signal power is -30 dBm. Observe that the main noise contributors are the input port and the input matching inductor L_{g1} and that the imput bias resistor does not appear among the main noise contributors. In fact, bias resistor layout is sufficiently long (and hence resistance sufficientely high) in order to minimise the noise contribution.

C. Stability

In order to evaluate the amplifier stability, two factors are taken into account: (1) Stern's stability factor Kf, and (2)

TABLE I
INTEGRATED NOISE SUMMARY.

Device	Noise Contribution [V^2]	% Of Total
PORT1	1.3×10^{-8}	58.84
L_{g1}	4.8×10^{-9}	21.51
M1	1.3×10^{-9}	6.15
L_s	1.1×10^{-9}	5.26
M2	3.8×10^{-10}	1.71
PORT2	3.4×10^{-10}	1.53
L_d	5.1×10^{-10}	2.28

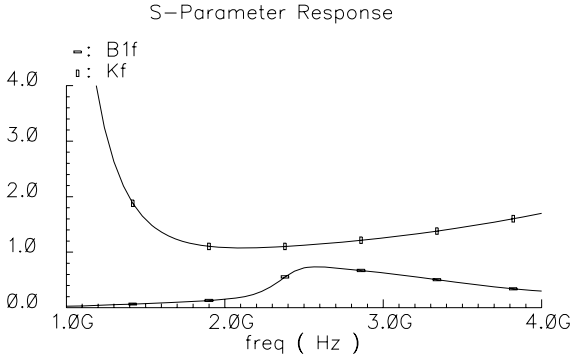

Fig. 7. The Stern Stability Factor.

$B1f = s_{11}s_{22} - s_{12}s_{21}$ [7]. The plots of Kf and $B1f$ are depicted in Fig. 7. Since, $Kf > 1$ and $B1f < 1$, the amplifier is unconditionally stable for all the load conditions.

D. Linearity

To estimate the amplifier linearity the 1-dB compression point is used as a figure of merit. The 1-dB compression point has been simulated in the case when the input power is -20 dBm. Fig. 8 shows that the output power gain drops 1 dB below the ideal gain when the input power is $-15,69$ dBm.

IV. CONCLUSION

In this paper, a new CMOS low noise amplifier in the 2.4 GHz ISM band using current reuse is proposed. Table II summarises the performance of the proposed design whereas Fig. 9 shows the amplifier layout. The proposed topology is suitable for ultra low-power applications since the estimated power consumption is 0.74 mW at 1.2 V supply voltage.

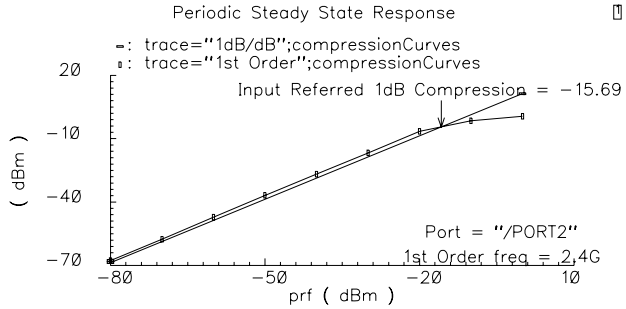

Fig. 8. The 1-dB Compression Point.

TABLE II
LNA PERFORMANCE.

Parameter	Value
Input matching (s_{11})	< -21 dB
Output matching (s_{22})	< -10 dB
Gain (s_{21})	13.3 dB
Reverse Isolation (s_{12})	-23 dB
P-1dB	-15.69 dBm
Noise Figure	< 2.28 dBm
Bias Current	0.61 mA
Supply Voltage	1.2 V
Power Consumption	0.74 mW
Area Occupation	0.235 mm^2

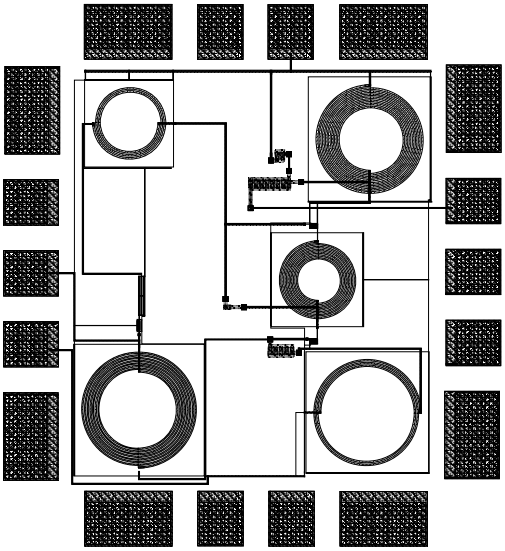

Fig. 9. Layout of the LNA.

Simulations using a UMC 0.13 μm process show a good noise figure of 2.28 dB, and excellent power gain (s_{21}) of 13.3 dB and linearity with a 1-dB compression point of -15.69 dBm.

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