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Vertical Silicon Nanowire MOSFET With A Fully-Silicided (FUSI) $NiSi_2$ Gate

Z. X. Chen, N. Singh, and D.-L. Kwong

***Abstract*—** This paper presents a vertical silicon nanowire *n*-MOSFET integrated with a CMOS-compatible fully-silicided (FUSI) $NiSi_2$ gate. Devices with nanowire diameter of 50nm show good electrical performance (SS < 70mV/dec, DIBL < 30mV/V, $I_{on}/I_{off} > 10^7$). Most significantly, threshold voltage tunability of about 0.2V is shown. Although threshold voltage remains low for the 50nm diameter device, it is expected to become more positive as nanowire diameter reduces.

***Keywords*—** $NiSi_2$ fully-silicided (FUSI) gate, vertical silicon nanowire (SiNW), CMOS compatible.

I. Introduction

THE Si nanowire (SiNW) MOSFET with gate-all-around (GAA) architecture shows promise in pushing the device scaling limits further [1-6]. The small nanowire diameter and excellent gate electrostatic control results in volume inversion of the channel, thus reducing short-channel effects, a big problem in scaling. However, as with many novel device architectures, the SiNW MOSFET has problems of its own. One major problem facing nanowire MOSFETs with SiO_2/Poly-Si gate stack is the lower than desired threshold voltage, V_T [2-4, 6]. Channel doping to correct the threshold voltage, V_T is difficult, given the narrow cylindrical nanowire. Carrier mobility is also impacted with higher channel doping. Gate work function tuning would thus make a better solution.

The CMOS-compatible fully-silicided (FUSI) gate process has been investigated to adjust the gate work function and thus the device V_T [6-11]. The gate work function and V_T were found to be easily tuneable through gate doping. In addition, the FUSI gate reduces the poly-Si gate depletion and resistance, enhancing device performance. NiSi FUSI gates have shown added advantage over other FUSI gate materials like $TiSi_2$ and $CoSi_2$ due to its lower anneal temperature, near-mid-gap work function, lower consumption of Si and ability to maintain low resistivity even at narrow gate lengths [12-13].

The Ni-FUSI gate has been demonstrated on SiNW MOSFETs [6] and FinFETs [9-11]. In this paper, we present a $NiSi_2$ FUSI gate implemented on vertical SiNW MOSFETs, which possess higher scaling potential, allowing much higher device density [4-5]. Apart from the good electrical performance, V_T is now tuneable.

The authors are with the Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), 11 Science Park Road, Science Park II, Singapore 117685 (phone: +65 6770 5633; e-mail: chenzx@a-star.edu.sg).

II. Device Fabrication

Three different gate splits were fabricated for comparison: (1) Phosphorous implanted poly-Si gate (poly-gate); (2) Unimplanted FUSI gate (FUSI gate); (3) Phosphorous implanted FUSI gate (tuned FUSI gate).

After nitride hard mask definition on *p*-type bulk-Si wafers (Fig. 1a), Si was etched, followed by sacrificial oxidation and grown oxide removal to form vertical SiNWs.

Vertical arsenic implantation and activation was done to dope the substrate and bottom of the nanowire (Fig. 1b). Isolation oxide was then formed by non-conformal deposition and DHF etch-back of HDP oxide (Fig. 1c). Gate stack of grown oxide (4.5nm) and α-Si (50nm) was then formed (Fig. 1d) and the α-Si was implanted and annealed with phosphorous from four orthogonal directions at a 30° tilt for the poly-gate and tuned FUSI gate devices. Another layer of isolation oxide was formed (Fig. 1e), exposing the poly-Si tip to be etched using RIE. The now exposed tip was implanted with arsenic from four orthogonal directions at a tilt of 45° (Fig. 1f). A layer of oxide is used to prevent the gate from being implanted.

A nitride spacer was formed to protect the nanowire tip to allow isolation oxide on the poly-Si to be stripped in DHF (Fig. 1g). After a gate pattern transfer (Fig. 1h) and a pre-clean, 30nm Ni was sputtered using PVD for FUSI gate and tuned FUSI gate devices (Fig. 1i). A single-step RTP anneal (440°C, 30s) was used to form the Ni-FUSI gate and un-reacted Ni removed in H_2SO_4:H_2O_2:H_2O solution (Fig. 1j). Finally, a low temperature (~400°C) back-end PMD and metallization process using Al was used to complete the fabrication (Fig. 1k).

A cross-sectional TEM image of a FUSI gate device is shown in Fig. 2. EDX done on the gate showed a Ni:Si ratio of 1:2. This is likely caused by a thinner PVD Ni layer deposited on the sidewalls of the gate creating a Ni-deficient $NiSi_2$ during silicidation. Other phases of Ni-FUSI gate can be formed by adjusting the Ni thickness and/or silicidation temperature.

III. Results and Discussion

The I_d-V_g curves of the vertical SiNW *n*MOSFETs are shown in Fig. 3a. The devices possess good characteristics of SS < 70mV/dec, DIBL < 30mV/V, and $I_{on}/I_{off} > 10^7$, but also has a low I_{on} (~300 μA/μm). This is due to the last implant not fully doping the nanowire under the hard mask, resulting in

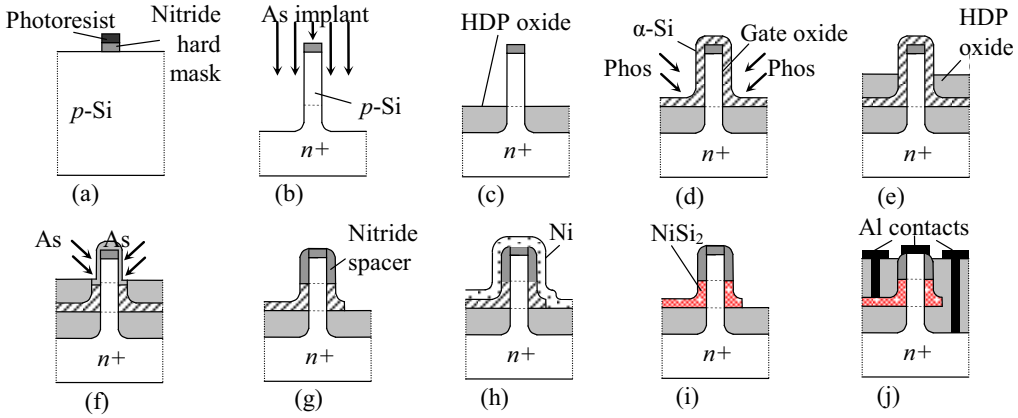

Fig. 1 Vertical SiNW FUSI gate MOSFET process flow. (a) Nitride hard mask etch, (b) Nanowire etch using deep RIE and vertical implantation of nanowire bottom. (c) HDP oxide non-conformal deposition and DHF etch-back. (d) Gate oxide growth, α-Si gate deposition and implantation. (e) HDP oxide deposition and DHF etch-back. (f) Isotropic dry etch of α-Si tip and nanowire tip implantation. (g) Formation of nitride spacer and oxide wet etch followed by gate patterning. (h) Ni deposition, (i) silicidation at 440°C and wet etch of unreacted Ni. (j) Aluminium contact formation.

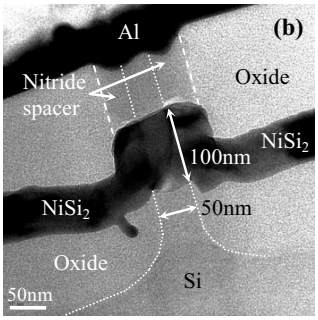

Fig. 2 Transmission electron microscope image of a $NiSi_2$ FUSI gate device with ~50nm diameter and ~100nm gate length.

high contact resistance. This can be rectified by fine tuning the implant conditions.

The devices also show V_T shifts relative to each other as can be seen in Fig. 3b. Most significantly, the FUSI gate has tuned the V_T by about +0.3V, resulting in a low positive V_T. Through the use of a FUSI gate, the V_T can also be adjusted within a 0.2V range. However, the FUSI process does induce some variations, especially for the tuned FUSI gate (σ=0.6). This could be due to small, unsilicided pockets of poly-Si at the oxide interface, which more likely to be present in doped gates where silicidation is slower.

As mentioned above, the FUSI gate increases V_T relative to the poly-gate device, but results in a V_T that is still low, leading to high I_{off}. However, as Fig. 3c shows, V_T increases with a decrease in nanowire diameter. So as nanowire diameter scales to sub-50nm, V_T will reach an ideal V_T without the need for gate implantation. But as diameter scales further, gate implantation would be required to correctly tune the now higher V_T.

IV. Conclusion

The $NiSi_2$ FUSI gate vertical SiNW *n*MOSFET has been presented, exhibiting good performance and proper V_T tuning via gate implantation. The device could give ideal V_T below 50nm diameter without any gate implantation but may require some tuning as diameter scales further.

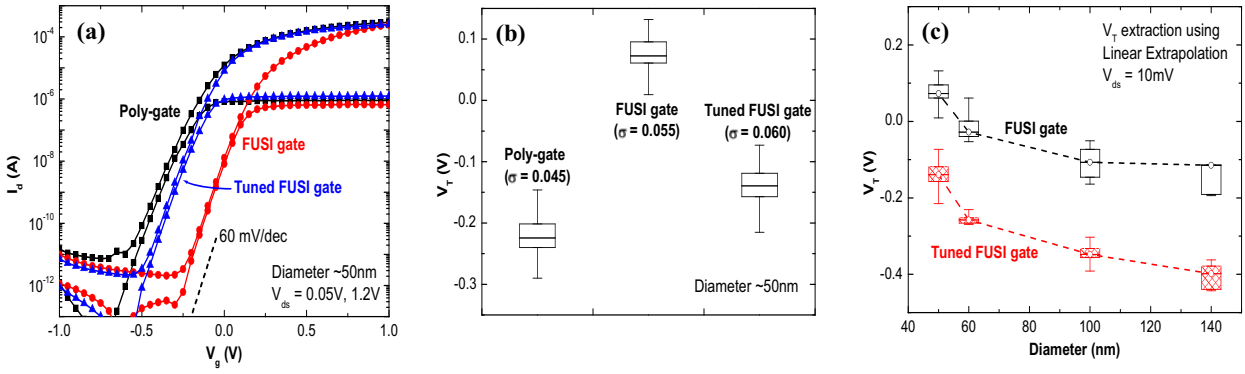

Fig. 3 (a) I_d-V_g plots of vertical SiNW *n*MOSFETs with poly-gate, FUSI gate, and tuned FUSI gate (I_{on} ~300μA/μm, SS < 70mV/dec, DIBL < 30mV/V, $I_{on}/I_{off} > 10^7$). (b) V_T distribution of more than 10 measured devices for each type of gate. (c) Box plots of the V_T distribution as SiNW diameter changes.

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REFERENCES

[1] S. Bangsaruntip, *et al.*, "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," in *IEDM Tech. Dig.*, 2009, pp. 297-300.

[2] N. Singh, *et al.*, "Si, SiGe nanowire devices by top-down technology and their applications," *IEEE TED,* vol. 55, no. 11, pp. 3107-3118, Nov. 2008.

[3] S. D. Suk, *et al.*, "High Performance 5nm radius Twin Silicon Nanowire MOSFET (TSNWFET) : Fabrication on Bulk Si Wafer, Characteristics, and Reliability," in *IEDM Tech. Dig.*, 2005, pp. 717-720.

[4] B. Yang, *et al.*, "Vertical silicon-nanowire formation and gate-all-around MOSFET," *IEEE EDL*, vol. 29, no. 7, pp. 791-794, Jul. 2008.

[5] J. Goldberger, *et al.*, "Silicon Vertically Integrated Nanowire Field Effect Transistors," *Nano Lett.,* vol. 6, pp. 973-977, 2006.

[6] Y. Jiang, *et al.*, "Nanowire FETs for low power CMOS applications featuring novel gate-all-around single metal FUSI gates with dual Φ_m and V_T tune-ability," in *IEDM Tech. Dig.*, 2008, pp. 869-872.

[7] H. Fukutome, *et al.*, "Cost-Effective Ni-Melt-FUSI Boosting 32-nm Node LSTP Transistors," in *Symp. VLSI Tech.*, 2008, pp. 150-151.

[8] J. A. Kittl, *et al.*, "Phase effects and short gate length device implementation of Ni fully silicided (FUSI) gates," *Microelectron. Eng.*, vol. 83, no. 11-12 pp. 2117-2121, Nov. 2006.

[9] T.-Y. Liow, *et al.*, "Strained N-channel FinFETs with High-Stress Nickel Silicide-Carbon Contacts and Integration with FUSI Metal Gate Technology", in *SSDM*, 2007, pp. 872-873.

[10] J. Kedzierski, *et al.*, "Fabrication of metal gated FinFETs through complete gate silicidation with Ni," *IEEE Trans. Electron Devices*, vol. 51, no. 12, pp. 2115-2120, Dec. 2004.

[11] S.-J. Choi, *et al.*, "Dopant-Segregated Schottky Source/Drain FinFET With a NiSi FUSI Gate and Reduced Leakage Current," *IEEE TED*, to be published.

[12] F. F. Zhao, *et al.*, "Thermal stability study of NiSi and $NiSi_2$ thin films," *Microelec. Eng.*, vol. 71, no. 1, pp. 104-111, Jan. 2004.

[13] H. Iwai, T. Ohguro, and S. Ohmi, "NiSi salicide technology for scaled CMOS," *Microelec. Eng.*, vol. 60, no. 1-2, pp. 157-169, Jan. 2002.