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Integration of Resistive Switching Memory Cell with Vertical Nanowire Transistor

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***Abstract*—**We integrate TiN/Ni/HfO_2/Si RRAM cell with a vertical gate-all-around (GAA) nanowire transistor to achieve compact $4F^2$ footprint in a 1T1R configuration. The tip of the Si nanowire (source of the transistor) serves as bottom electrode of the memory cell. Fabricated devices with nanowire diameter ~ 50nm demonstrate ultra-low current/power switching; unipolar switching with 10μA/30μW SET and 20μA/30μW RESET and bipolar switching with 20nA/85nW SET and 0.2nA/0.7nW RESET. Further, the switching current is found to scale with nanowire diameter making the architecture promising for future scaling.

***Keywords*—**RRAM, 1T1R, gate-all-around FET, nanowire FET, vertical MOSFETs

I. Introduction

RESISTIVE RAM (RRAM) has been studied extensively in recent years due to its potential being the solution to the scaling issues in current charge-trapping based non-volatile memory (NVM) [1-6]. Superior data retention, high speed program/erase and low operating voltages make it suitable particularly for embedded NVM application using standard CMOS BEOL process [1-6]. In 2010, RRAM cell integrated with a 3-dimensional (3D) vertical bipolar junction transistor (BJT) is demonstrated to have $4F^2$ footprint [3]. It was the first attempt to use transistor (other than diode) as the select device with $4F^2$ density. However, BJT has higher leakage current and it may complicate the process flow if it is to be implemented along with CMOS logic. Therefore, a more direct way to realize the $4F^2$ density is to integrate the memory cell on a vertically stacked MOSFET.

In this letter, for the first time, we present the 1T1R integration of RRAM cell with vertical nanowire (VNW) CMOS to achieve $4F^2$ footprint for large scale storage usage. A full CMOS compatible process flow, with only one additional mask layer, is used to realize this self-aligned 1T1R structure. Excellent device characteristics and current scalability is obtained with this structure. Ultra-low current switching is presented for low power applications in portable electronic devices.

II. Device Fabrication

Vertical gate-all-around (GAA) Si nanowire (NW) MOSFET was chosen to be the selection device because of its high scaling potential, low off state current and $4F^2$ footprint [7]. The RRAM cell was directly formed on top of nanowire FETs without occupying any planar space. The tip of the Si nanowire serves directly as the bottom electrode of the RRAM cell. The 1T1R structure uses gate poly line as the word line (WL) and metal line connecting the top electrode of RRAM as the bit line (BL).

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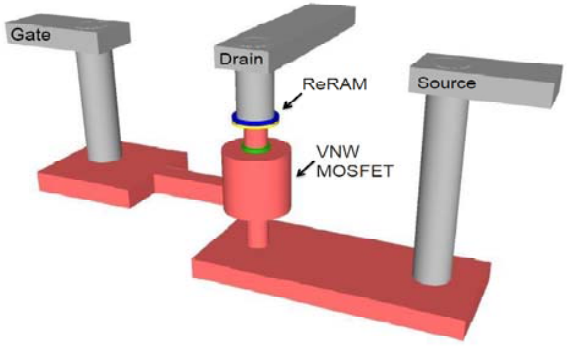


Fig. 1 Schematic showing the three-dimensional view of the VNW 1T1R architecture with RRAM cell directly built on top of the Si nanowire

The select line (SL) is the active pad. The 3D schematic of the fabricated device is displayed in Fig. 1. The device fabrication process flow is presented in Fig. 2. The vertical NW transistor fabrication process steps follow the same as introduced in [7], as in Figs. 2(a)-(g). After forming the transistor, wafer was planarized by oxide deposition and chemical-mechanical planarization (CMP). The nitride hard mask was then removed to expose the doped nanowire tip (source terminal). The tip for the smallest design had diameter of 50 nm. The nitride spacer was then formed to protect the exposed nanowire sidewalls from making contact to RRAM cell. Physical vapor deposition (PVD) HfO_2, Ni and TiN were deposited as the RRAM dielectric and top electrode layers, followed by cell lithography and etching (Fig. 2(h)). This lithography uses the same mask layer as the nanowire. The fabrication processes were completed with pre-metal oxide deposition (PMD), contact formation and Al metallization.

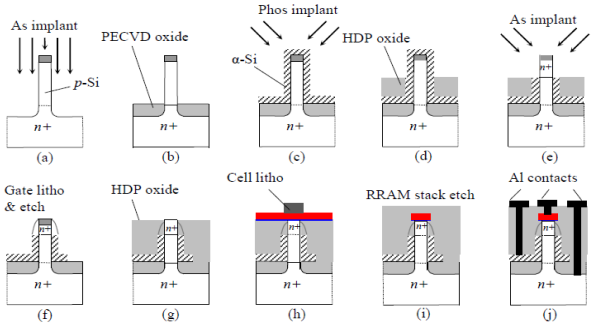


Fig. 2 Fabrication process flow of the vertical NW 1T1R cell: (a) bottom implantation after nanowire definition; (b) after isolation oxide; (c) gate oxide/α-Si stack deposition, followed by gate shallow implantation; (d) wet etch back of HDP oxide to form etch mask of α-Si exposed from wire tip; (e) α-Si wet etch and top angle implantation; (f) 1st nitride spacer and oxide strip, followed by gate litho and etching; (g) HDP oxide deposition, CMP to stop on nitride hard mask, oxide wet etch back and nitride removal; (h) cell litho to define the top electrode after 2nd nitride spacer, dielectric and metal deposition, same nanowire mask layer used; (i) PMD and contact formation; and (j) metallization with Al

III. Results and Discussion

The fabricated 1T1R cell has two modes of operations: unipolar (Mode-I) and bipolar (Mode-II), as displayed in Fig. 3 for a 50 nm wide nanowire transistor. The current compliance during forming process was kept at 1.0μA for Mode I and 10nA for Mode II. The forming voltage was about 6.5V. High value could be due to the formation of native oxide interfacial layer at the HfO_2/Si interface. However, the RESET current is as low as 20μA (mode I) and 200pA (mode II), respectively. The word line voltage is kept at 0V during the SET/RESET as the nanowire transistors with poly silicon gate are normally ON devices [7]. From a control wafer without RRAM cell, a drive current of 25μA at an operating voltage of 1.2V is obtained for a 37nm diameter nanowire transistor (not shown). The nanowire transistor could supply enough current to the memory cell owing to the small size of the memory cell [4]. Fig. 4(a) shows the unipolar mode switching characteristics for n^+ doped nanowire (without FET) and 1T1R cell of different nanowire diameters. The RESET current scales with nanowire diameter and is also proportional to transistor drive current. The nanowire transistors in this case limit the RESET current [8]. Fig. 4(b) depicts the ultralow current bipolar mode switching for 100 DC cycles. The switching power for SET is 85nW and RESET is 0.7nW (in comparison to 10μA/30μW and 20μA/30μW for unipolar mode). The DC endurance cycles and room temperature (RT) retention characteristics for unipolar and bipolar mode are presented in Fig. 5. Well defined ON/OFF window with more than 50 and 10 times difference in magnitude is observed after DC cycling for mode I and II, respectively. There is no degradation of the resistance window at room temperature after more than 3000 times read disturbance.

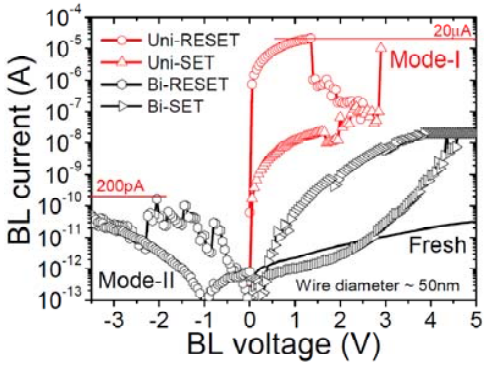
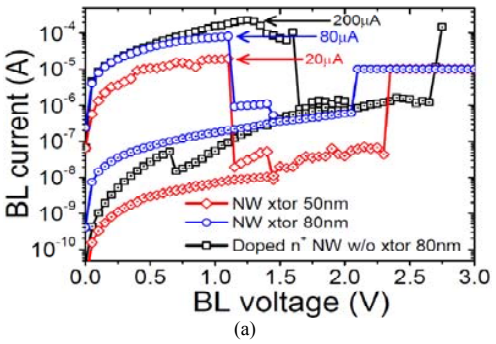
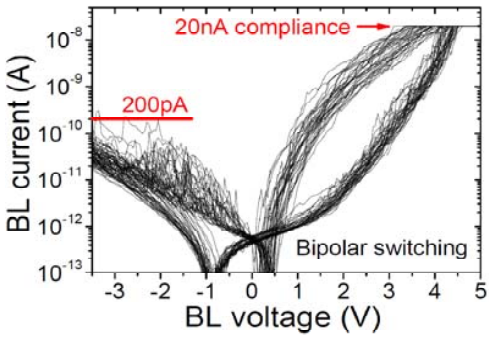


Fig. 3 Memory cell operations under unipolar and bipolar modes at V_{WL}=V_{SL}=0V. VNW transistors supplied sufficient drive current for unipolar operations



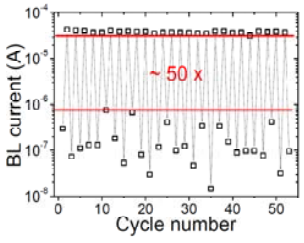
(a)



(b)

Fig. 4 (a) Reset current scales with NW diameter (i.e., drive current & bottom electrode area) under unipolar mode operations. (b) Ultra-low RESET current under bipolar mode operations. SET power < 85nW, RESET power < 0.7nW

The origin of unipolar switching is the formation and thermal dissolution of conductive filament in NiO layer at Ni/HfO_2 interface [9]. For bipolar switching, the soft forming process creates defects in HfO_2 with much lower density. Current-voltage fitting confirmed the presence of Schottky barrier at the broken down HfO_2 and Si interface. For positive V_{BL}, electrons overcome smaller barrier to jump from Si to traps in HfO_2 as compared with negative V_{BL}. This creates the asymmetric current conduction as shown in Fig. 4(b). At the TiN/Ni/HfO_2 interface, another barrier which can be formed/ruptured by RESET/SET is responsible for the switching between high and low resistance states.



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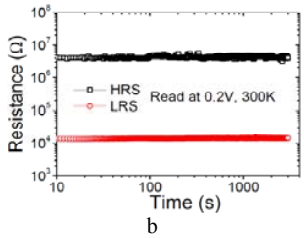

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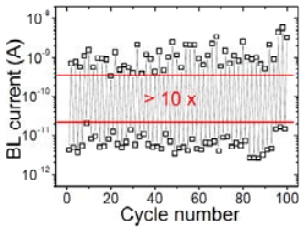

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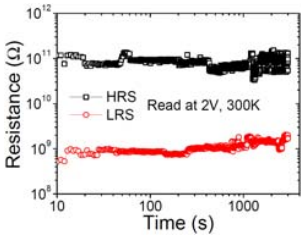

d

Fig. 5 50 DC cycles of the ReRAM cell under unipolar mode operation (V_{BL}=0.2V); and (b) its RT retention characteristics. (c) 100 DC cycles of the ReRAM cell under ultralow bipolar mode operation (V_{BL}=2V); and (d) its RT retention characteristics

IV. Conclusion

Full CMOS compatible integration of RRAM with vertical GAA nanowire transistor is demonstrated with $4F^2$ footprint. Excellent current scalability is achieved with reduced nanowire diameters, making it ready for advanced technology nodes. The presented vertical nanowire CMOS platform with ultralow switching current is promising for high-density low power RRAM integrations, including embedded memory.

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