

A 16Kb 10T-SRAM with 4x Read-Power Reduction

Pardeep Singh, Sanjay Sharma, Parvinder S. Sandhu

Abstract—This work aims to reduce the read power consumption as well as to enhance the stability of the SRAM cell during the read operation. A new 10-transistor cell is proposed with a new read scheme to minimize the power consumption within the memory core. It has separate read and write ports, thus cell read stability is significantly improved. A 16Kb SRAM macro operating at 1V supply voltage is demonstrated in 65 nm CMOS process. Its read power consumption is reduced to 24% of the conventional design. The new cell also has lower leakage current due to its special bit-line pre-charge scheme. As a result, it is suitable for low-power mobile applications where power supply is restricted by the battery.

Keywords—A 16Kb 10T-SRAM, 4x Read-Power Reduction

I. INTRODUCTION

CMOS SRAM memory has been and will continue to play a critical role in modern microprocessors. Due to its complex 6T structure, as shown in Fig. 1, SRAM cache is one of the most area-consuming components in the state-of-the-art system-on-chip (SoC) [1]. According to the 2002 International Technology Roadmap for Semiconductors (ITRS 2002), memory chip will occupy 90% of the chip area by 2013. As a result, SRAM cell transistors normally use minimum width-to-length ratios to meet this stringent area constrain. This, coupled with the steadily increasing fluctuations in transistor parameters (e.g., threshold voltage V_{th}) and process parameters (e.g., doping level) as device dimensions and supply voltage scale down in the nanometer regime, leads to the urge to maximize the cell stability for future technology. Another major concern is the power consumption of high density SRAM. Eqs. (1) and (2) represents a simplified model of total power consumption of an SRAM which is inclusive of active and passive power P_{active} and $P_{passive}$, respectively [2]. Assuming that the SRAM macro in consideration has m columns and n rows, its standby or leakage power will be proportional to the leakage current per cell, as shown in Eq. (2). As a result, it is desirable to have as low leakage current as possible as this is becoming a dominant component of total power consumption in sub-100 nm CMOS technologies [3-5].

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The second component is P_{active} which is consumed when a SRAM is read or written. During these operations, a row is chosen by triggering one of the WLs high and hence the access transistors (N3 and N4 in Fig. 1) of all the cells on that row will be turned on. Each cell then draws an active current i_{cell} , hence a current of $m \times i_{cell}$ is consumed. Therefore, it is necessary to partition the macro in to smaller sub-macros in order to reduce this component. During these active cycles, the decoder and other peripheral circuits such as sense amplifier and write driver also contribute a significant amount of power consumption, as shown in Eq. (2).

$$P_{stand\ by} = m \times n \times i_{hold} \times VDD \quad (1)$$

$$\begin{aligned} P_{active} &= I_{DD} VDD \\ &= (I_{core} + I_{decoder} + I_{peripheral}) VDD \\ &= \{ [m \times i_{cell} + m(n-1) i_{hold}] + I_{decoder} + I_{peripheral} \} VDD \end{aligned} \quad (2)$$

In this work, we focus on the first component of the active power, i.e. I_{core} by redesigning the memory cell. We propose a new 10T SRAM cell and a new bit-lines pre-charge scheme (BL and BLB, Fig. 2) that can reduce $m \times i_{cell}$ component into $1 \times i_{cell}$ and thus I_{core} is drastically reduced. The new cell also offers a lower leakage and hence is suitable for applications where the system is in standby mode in majority of the time.

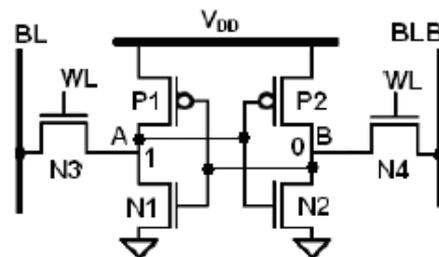


Fig. 1 Conventional 6T SRAM cell

II. THE NEW 10T SRAM CELL

Fig. 2 shows the schematic of the proposed cell with separate read and writes ports. It consists of four pMOSs (P1–P4) and six nMOSs (N1–N6). Like the conventional SRAM, P1, N1 and P2, N2 form a cross-coupled inverters flip-flop which has two stable states to store either a ‘0’ or a ‘1’. Fig. 3 illustrates a simplified read data path of the proposed design with two BL pre-charge transistors (N11,N12), pull-up transistors (P10-P12), a bit-line sense amplifier and four data-

lines driving transistors (P13-P16). During standby, both BLs are pre-charged to ground, as shown by the light blue lines in Fig. 4. When a read operation is activated, a specific memory cell is chosen by its corresponding Read Word Line (RWL) and Column Select (CS) signals (Fig. 3). Consequently, N11 and N12 are turned off to release the BLs. As P10-P13 are turned on, they charge the BLs up from ground level

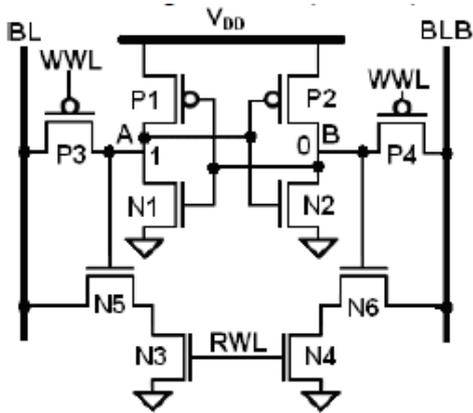


Fig. 2 Proposed 10T cell with separate write/read ports.

From now on, for the ease of explanation, assuming that the chosen cell stores a '0', N5 is off whereas N6 is on. Since RWL is trigger high, a small current I_{cell} flows from BLB to ground, causing V_{BLB} to rise slower than V_{BL} , i.e. $V_{BLB} < V_{BL}$. Thus, V_{GS} of P11 is larger than that of P12 and P11 sources a higher current than P12. Consequently, V_{BL} continues to rise with a higher rate than V_{BLB} and quickly creates a large voltage gap between these two lines. The sense amplifier is then turned on to sense this voltage difference and amplify it to intermediate outputs C and D, as shown in Fig. 3 and 4. Since C is pulled to ground while D is pushed to VDD, P15 is turned on and P16 is cut-off. P15 sources a current to DLB and pushes it to a high voltage level while DL remains unchanged. A simple buffer is then used to provide full CMOS logic level outputs, as shown in Fig. 2 and Fig. 4. Although the RWL signal turns on N3 and N4 of all the cells in the same row, the BLs of the other column are kept at ground level and hence no I_{cell} flows into the other cells on the accessed row. Thus, power dissipated within the SRAM core is mainly consumed by the sense amplifier and a hefty amount of current is saved. The proposed SRAM design has a similar write operation as the conventional design. When data is transferred to the BLs, the Write Word Line (WWL) turns on the access transistors of the cells and data is written. However, since the precharge level of BLs is ground, pMOS transistors (P3 and P4 in Fig. 2) are used to access the memory instead of nMOS transistors (N3 and N4 in Fig. 1). This results in a slightly smaller cell current during a write and hence the proposed design has a slower write delay and a lower write power when compared to the conventional 6T

design (discussed in Section III). Fig. 5 illustrates the waveforms of a several nodes of the proposed design during a write operation. The proposed design has 24% layout area overhead when compared to the conventional 6T layout due to four additional nMOS transistors and the wiring of the additional RWL. However, as technology scales down, excessive fabrication fluctuations require 6T design to use larger transistor size to maintain its stability [6]. Thus, the 10T design has its advantage as the area overhead can be reduced when minimum size transistors can be used while maintaining its high stability

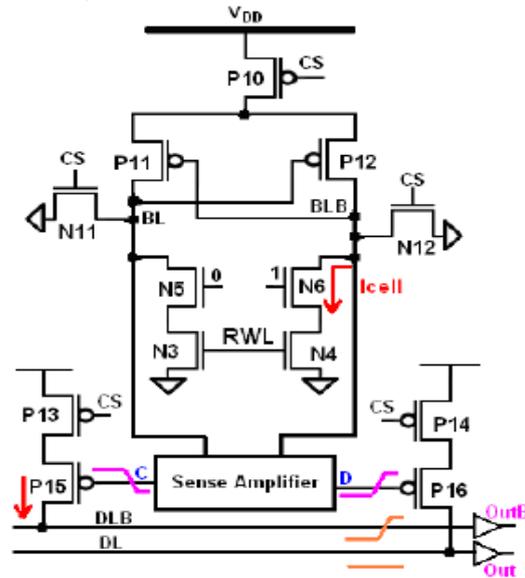


Fig. 3 Data path in the read cycle of the proposed SRAM.

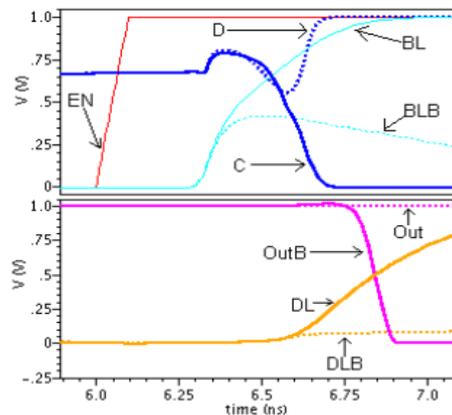


Fig.4 Waveforms of several nodes during a read cycle.

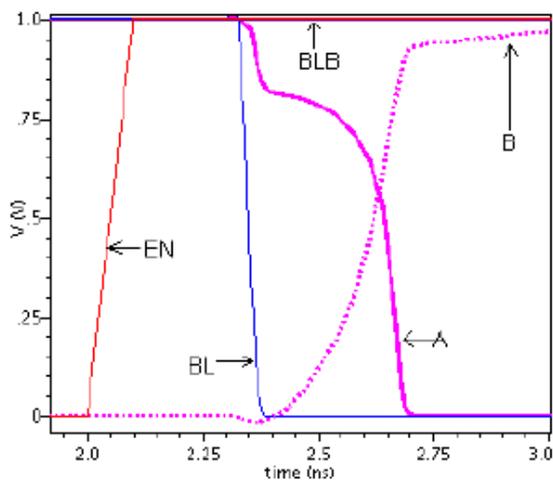


Fig. 5 Waveforms of several nodes during a write cycle

III. PERFORMANCE COMPARISON

A. Dynamic Noise Margin

Static Noise Margin (SNM) is the most popular measures to evaluate the stability of the memory cell [7-9] as it indicates how much noise is needed to malfunction the cell content under the worst case scenario. However, recent works on cell stability have pointed out that SNM is only a special case under a broader class of Dynamic Stability (DS or Dynamic Noise Margin – DNM) in which noise pulse width (NPW) extends to infinity [10-12]. In this work, we performed a simple DNM analysis of the proposed design and the conventional 6T cell using different NPW at 400 C and 1000 C, respectively. Simulation results are presented in Fig. 6 and strongly agree with the conclusion in Ref. [10, 11]. Both designs have very high margin when the NPW is exceptionally short, i.e. about 10 ps but drop by more than 70% when the pulse width increase to 100 ps. For example, at 400 C, 10 ps NPW, the DNM of the 10T and 6T cells are 1460 mV and 820 mV, respectively. On the other hand, these

DNMs saturate and approach their SNM values of 390 mV and 198 mV, respectively with NPW higher than 100 ps. This has affirmed that the proposed design has about 2X more stability when compared to the conventional 6T design dynamically and statically.

B. Cell Leakage

Leakage current is one of the major concerns in nano-scale SRAM where most of the transistors are in the standby mode [13]. Although the proposed 10-T cell has more transistor count, our bit-line pre-charge voltage of 0V incurs no additional leakage to the cell. Furthermore, the pull-down transistors N1 and N2 are smaller than those in the conventional cell, hence its leakage is reduced. Fig. 7 compares the leakage current of the two designs at various operating temperature. The proposed cell's leakage is only about 73% of that of the conventional 6T cell. For example, at 600

C, the 10T and 6T SRAM have a leakage current of 49 pA and 67 pA, respectively.

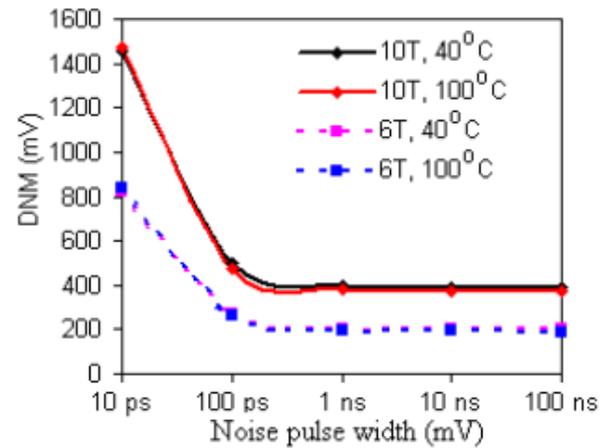


Fig. 6 Dynamic Noise Margin of the conventional and the new 6T cells versus the cell ratio and the access transistor's width variations.

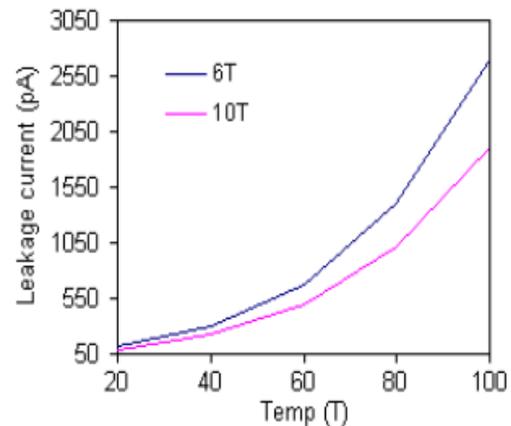


Fig.7. Leakage current comparison of the two designs against the temperature variation.

C. Read/Write performance

Two 128x128 SRAM macros have been implemented in a standard 65 nm CMOS process from CHRT using the conventional 6T and the 10T cells. Both macros have identical address decoders, data-line drivers and sense amplifier design. Extensive Read/Write operations have been simulated at 400 C to evaluate the performance of the newly proposed cell. All results are recorded at 250 MHz and 500 MHz operating frequency, as shown in Table III. It is apparent that at both operating frequencies, the proposed design has a significantly less read power consumption. This is because only one cell is turned on instead of all the cells in one row in the conventional design. At 250 MHz, the 6T SRAM macro has 4X read power consumption when compared to that of the new design. Our design has slightly slower read delay which is about 40 ps longer. The new design's write power is also reduced by 30% when compared to conventional 6T design.

Relative performance of the two macros at two different operating frequencies is summarized in Table I.

TABLE I
SUMMARY OF THE PERFORMANCE OF THE TWO SRAM MACROS.

	10T SRAM macro	6T SRAM macro
250 MHz	Read Power: 0.78 mA Read Delay: 820 ps Write power: 2.0 mA Write delay: 600 ps Peak current: 10.9 mA	Read Power: 3.25 mA Read Delay: 780 ps Write power: 3.3 mA Write delay: 580 ps Peak current: 10.1 mA
500 MHz	Read Power: 1.6 mA Read Delay: 790 ps Write power: 3.2mA Write delay: 600 ps Peak current: 11.8 mA	Read Power: 4.4 mA Read Delay: 760 ps Write power: 4.5 mA Write delay: 600 ps Peak current: 12.7 mA

Fig.8 illustrates the breakdown of read power consumption.

As introduced in section I, it consists of two components: Core dissipation and peripheral dissipation. Theoretically, by turning on only one cell during a read operation power dissipation of the proposed design would be 1/128 of that of the conventional design. However, some circuit components also draw currents when the core is activated such as the RWL or the CS. These are short pulse currents and quickly diminish after a few tens of picoseconds. This explains why at 500 MHz, the power reduction within the core is 8X whereas that at 250

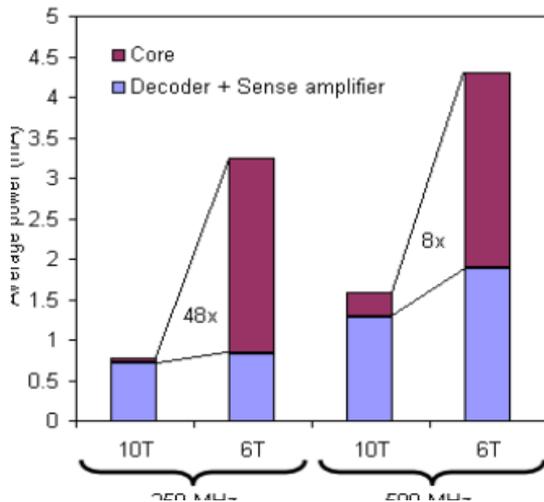


Fig.8 Average read power of the two designs during a read cycle

MHz is 48X. Despite the fact that these numbers are far below the optimum value of 128, our proposed design has made a measurable power reduction within the core. This

implies that power consumed due to half-access cells during the read operation is no longer a design bottleneck and circuit designers can partition the macro differently with more cells per row, hence its layout is more efficient and can be used to compensate the area overhead induced by the larger 10T cell layout.

IV. CONCLUSION

A novel 10T SRAM cell has been proposed and analyzed. It has successfully separated the write and read operations of the SRAM and hence fully solved the noise margin problem during the read cycle. As a result, its noise margin is 2X higher than that of the conventional 6T design. Concurrently, it reduces 76% of the total read power. Considering the active current within the core, the proposed design offers more than 90% reduction. Its write and read delay are also compatible to that of the conventional 6T. In addition, its leakage is 27% lower. In view of the above-mentioned advantages, it can be concluded that the new design is a better choice for applications that require ultra low-power and highly stable memory. The advantage of the proposed design will be even more significant for smaller technology nodes and lower power supply voltage.

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