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Quantum Dot Cellular Automata Based Effective Design of Combinational and Sequential Logical Structures

Hema Sandhya Jagarlamudi, Mousumi Saha, and Pavan Kumar Jagarlamudi

***Abstract*—**The use of Quantum dots is a promising emerging Technology for implementing digital system at the nano level. It is effecient for attractive features such as faster speed , smaller size and low power consumption than transistor technology. In this paper, various Combinational and sequential logical structures - HALF ADDER, SR Latch and Flip-Flop, D Flip-Flop preceding NAND, NOR, XOR,XNOR are discussed based on QCA design, with comparatively less number of cells and area. By applying these layouts, the hardware requirements for a QCA design can be reduced. These structures are designed and simulated using QCA Designer Tool. By taking full advantage of the unique features of this technology, we are able to create complete circuits on a single layer of QCA. Such Devices are expected to function with ultra low power Consumption and very high speeds.

***Keywords*—**QCA, QCA Designer, Clock, Majority Gate

I. Introduction

IN the past few decades, complementary metal-oxide semiconductor (CMOS) technology has consistently played a vital role in implementing high-density, high-speed and low-power very large scale integrated systems. It provided the required dimensional scaling to support the integration. However, several studies have predicted that these technologies approaching its fundamental physical limits [4], [5] and the current silicon transistor technology faces challenging problems. Quantum dot cellular automata (QCA) is one of the attractive alternatives. QCAs were introduced in 1993 by lent et al, and experimentally verified in 1997. It is expected to achieve high device density, extremely low power consumption and very high switching speed.The QCA offers a new transistorless computing paradigm in nanotechnology. QCA structures are constructed as an array of quantum cells within which every cell has an electrostatic interaction with its neighboring cells. QCA applies a new form of computation, where polarization rather than the traditional current, contains the digital information. In this trend, instead of interconnecting wires, the cells transfer the information throughout the circuit [2].The fundamental QCA logic primitives are the three input Majority gate, wire and inverter [4]-[7]. QCA digital architectures are combination of these. The basic logic elements used in this technology are the inverter and the majority gate. The other logical structures are designed using these basic elements.The paper is organized as follows, in section 2, describes QCA overview, section 3 explains QCA Clocking. In section 4, explains QCADesinger Tool and section 5, provides different logical structers implementaion using majority gates and also comparision. Section 6, presents simulation results followed by conclusion in section 7. Section 8 is of references.

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II. QCA Overview

The QCA cell consists of four quantum dots positioned at the corners of a square. The cell contains two extra mobile electrons, which are allowed to tunnel between neighboring sites of the cell. Coulombic repulsion causes the electrons to occupy antipodal sites within the cell. These two bistable states result in cell polarizations of P = +1(binary 1) and P = -1(binary 0) and one Null state , P=0 as shown below in Fig.1.

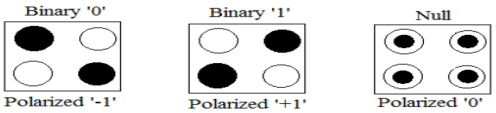


Fig. 1 QCA Cell Polarization

The power needed to perform the polarization changes in cells (that support logic operations) is supplied by the clock signal .

A. QCA Logic Devices

In a QCA wire, the binary signal propagates from input to output because of the electrostatic interactions between cells. The propagation in a 90° QCA wire is shown in Fig. 2. Another is 45° QCA wire, in Fig.3. In this case, the propagation of the binary signal alternates between the two polarizations.

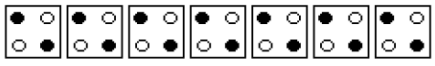
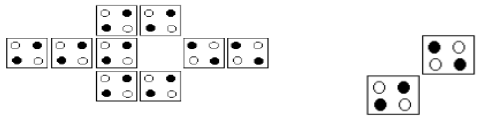


Fig. 2 QCA wire 90 °

Fig. 3 QCA wire 45 °

The electrostatic interaction is inverted, as the quantum dots corresponding to different polarizations are misaligned between the cells as in Fig. 4(a). There are several inverter types [1], [5]. Inverter of two cells is shown in Fig. 4(b).



(a) (b)

Fig. 4 (a) QCA Inverter (b) 2-cell QCA Inverter

The fundamental QCA logical device, a 3 input majority gate, shown in Fig.5. from which more complex circuits can be built. The central cell, labeled the device cell, has three fixed inputs, labeled A, B, and C. The device cell has its lowest energy state if it assumes the polarization of the majority of the three input cells. The inputs to a particular device can come from previous calculations or be directly fed in from array edges.

$M(A,B,C)= AB + BC + CA.$

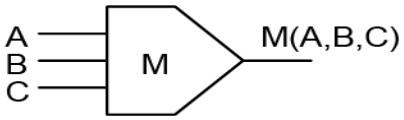


Fig. 5 Majority Gate

B. QCA Defects

The types of defect that are likely to occur in the manufacturing of QCA devices are illustrated in Fig. 6 .

They can be categorized as follows:

i). In a cell displacement defect, the defective cell is displaced from its original position. For example, in Fig. 6(b), the cell with input B is displaced to the north by Δ nm from its original position.

ii). In a cell misalignment defect, the direction of the defective cell is not properly aligned. For example, in Fig. 6(c), the cell with input B is misaligned to the east by Δ nm from its original position.

iii). In a cell omission defect, the defective cell is missing as compared to the defect-free case. For example, in Fig. 6(d), the cell with input B is not present.

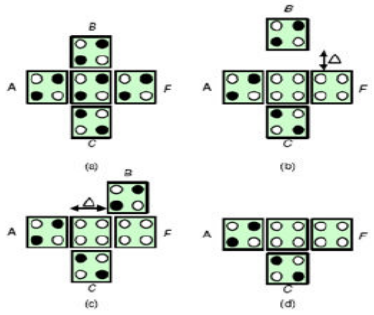


Fig. 6 (a) Defect-free majority gate, (b) displacement defect, (c) misalignment defect, and (d) omission defect.

III. Clocking

The QCA circuits require a clock, not only to synchronize and control information flow but also to provide the power to run the circuit since there is no external source for powering cells (serial add, shifter). With the use of four phases clocking scheme as shown in Fig.7 in controlling cells, QCA processes and forwards information within cells in an arranged timing scheme. This clocking method makes the design of QCA different from CMOS circuits [12]-14].

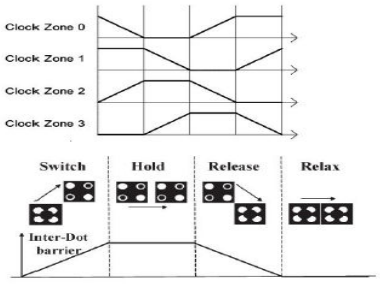


Fig. 7 The four phases of QCA Clock

IV. QCA Designer

QCA Designer is capable of simulating complex QCA circuits on most standard platforms. Initially developed at the ATIPS Laboratory, University of Calgary, QCA Designer has attracted some important new developers, including top researchers from the University of Notre Dame. The current version of QCA Designer has three different simulation engines included. The first is a digital logic simulator, which considers cells to be either null or fully polarized. The second is a nonlinear approximation engine, which uses the nonlinear cell-to-cell response function to iteratively determine the stable state of the cells within a design. The third uses a two-state Hamiltonian to form an approximation of the full quantum mechanical model of such a system. Each of the three engines has a different and important set of benefits and drawbacks. Additionally, each simulation engine can perform an exhaustive verification of the system or a set of user-selected vectors. [9]-[11].

QCA logic and circuit designers require a rapid and accurate simulation and design layout tool to determine the functionality of QCA circuits. QCA Designer gives the designer the ability to quickly layout a QCA design by providing an extensive set of CAD tools. As well, several simulation engines facilitate rapid and accurate simulation. One of the main problems in implementing more accurate simulations is the lack of experimental data for QCA systems with a large number of cells.

V. QCA Implemetation

The AND and OR gates are realized by fixing the polarization to one of the inputs of the majority gate to either P = 1 (logic 0) or P = 1 (logic 1) as shown in Fig.8.

Fig. 8 AND Gate and OR Gate Layout

Since NAND and NOR are complements of AND and OR. Hence, are designed by adding an inverter to respective structures as shown in Fig.9.

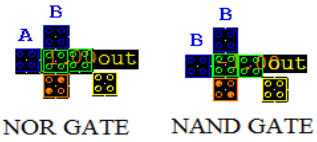


Fig. 9 NOR Gate and NAND Gate Layout

For XOR gate, if inputs are different , then ouput is HIGH, else LOW. In case of, XNOR gate, the output is complement of XOR gate. The layouts are designed with less number of cells as shown in Fig.11, Fig.10.

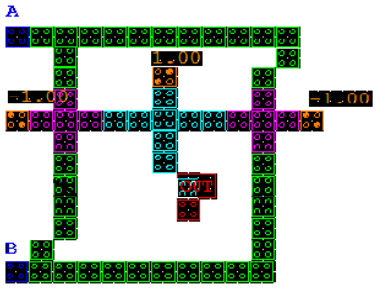


Fig. 10 XNOR Gate Layout

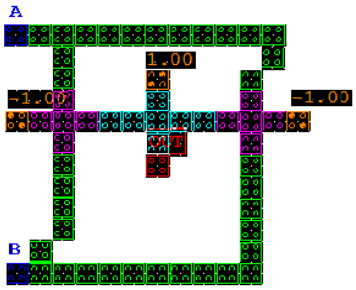


Fig. 11 XOR Gate Layout

Half Adder logical operation is, two inputs A,B when anded gives carry and xored gives sum. It is realized in simplest way as shown in Fig.12.

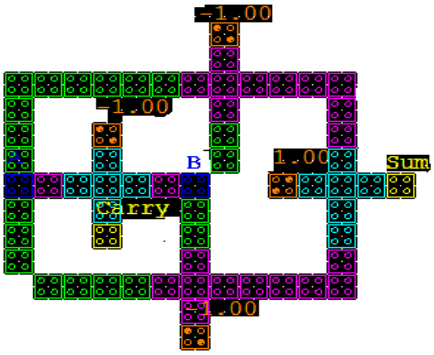


Fig. 12 Half Adder Layout

Not only combinational circuits, but also sequential circuits can be designed using QCADesigner Tool. The Fig.13, shows the layout of SR Latch. The SR Latch consists of inputs SET(S), RESET(R) and output Q. The boolean expression is as follows:

$$Q_{n+1} = S + \bar{R}Q_n$$

The SR Flip-Flop in Fig.14 and D Flip-Flop in Fig.15 are designed according to Boolean expression obtained from truth table by K-Map.

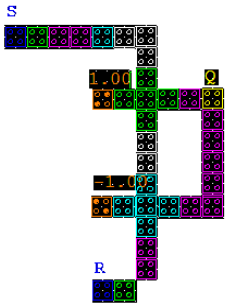


Fig. 13 SR Latch

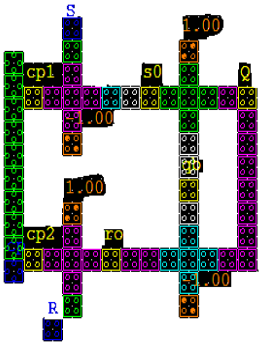


Fig. 14 SR Flip-Flop Layout

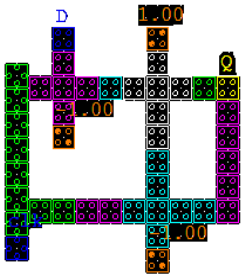


Fig. 15 D Flip-Flop Layout

VI. Simulation Results

With QCADesigner ver.2.0.1, the logical structure functionality is verified. Bistable approximation is done where Cell size is 20nm, Scale factor for all cells is '1', Clock high is 9.8e-22J, Clock low is 3.8e-23J,Upper Threshold of 0.5000, 12000 number of samples, Lower Threshold of -0.5000, Inputs are merged into single Bus .

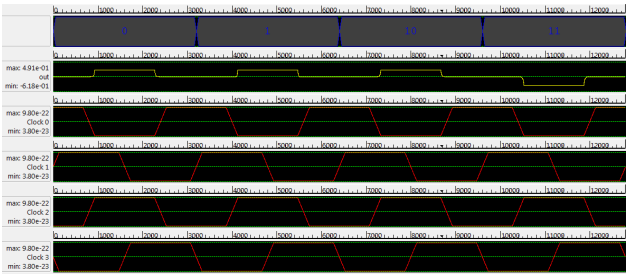


Fig. 16 Simulation result of NAND Gate

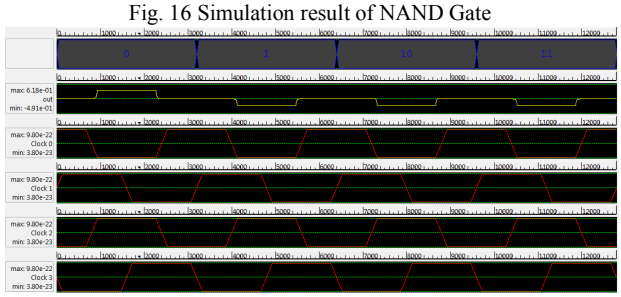


Fig. 17 Simulation result of NOR Gate

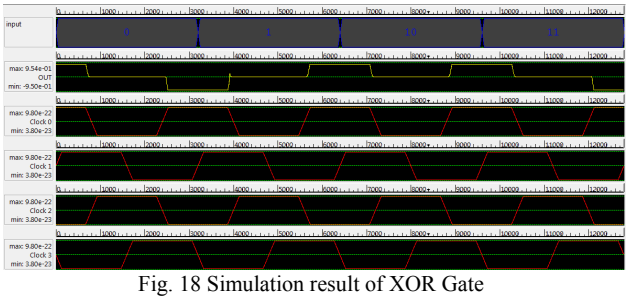


Fig. 18 Simulation result of XOR Gate

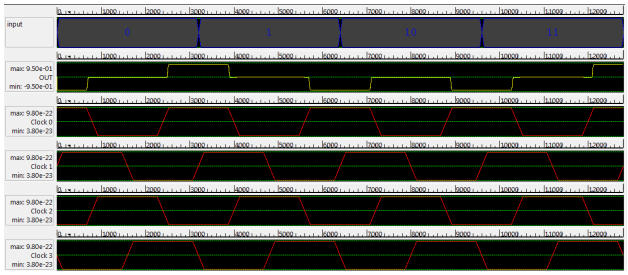


Fig. 19 Simulation result of XNOR Gate

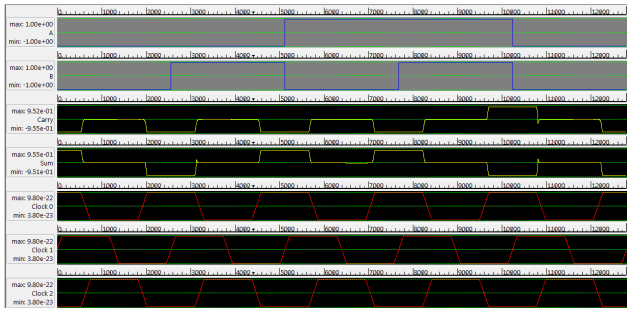


Fig. 20 Simulation result of Half Adder

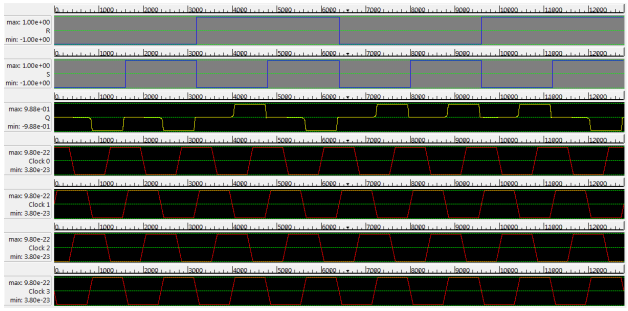


Fig. 21 Simulation result of SR Latch

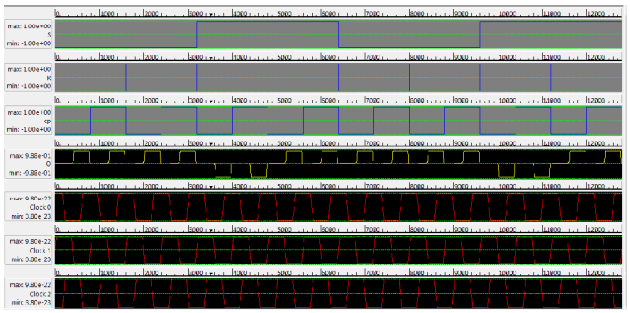


Fig. 22 Simulation result of SR Flip-Flop

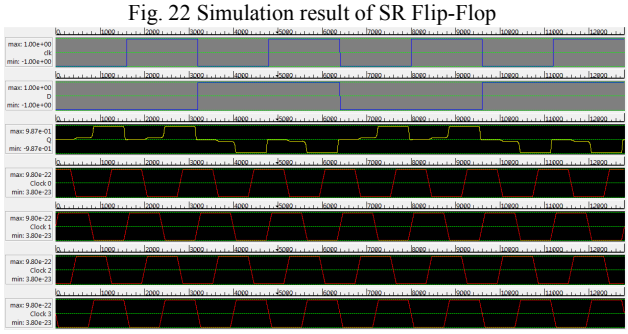


Fig. 23 Simulation result of D Flip-Flop

VII. Observations

For Half Adder logical structure 61 cells are required. In case of, SR Latch 34 cells are needed to design. In both the cases area consumption is less which can be observed from Fig.12, Fig.13. TABLE I provides the comparision list of this paper work and previous work.

TABLE I
COMPARISION

Logical Structures	Previous Structure		New Structure	
	Cells	Area	Cells	Area
NAND	7 cells	63nm x 103nm	6 cells	80nm x 60nm
NOR	7 cells	63nm x 103nm	6 cells	80nm x 60nm
XOR	64 cells	300nm x 220nm	54 cells	290nm x 220nm
XNOR	65 cells	300nm x 220nm	56 cells	290nm x 220nm
D Flip-Flop	68 cells	300nm x 280nm	42 cells	202nm x 200nm
SR Flip-Flop	76 cells	382nm x 240nm	60 cells	260nm x 300nm

VIII. Conclusion

The Combinational and Sequential logical structures using QCA have been realized effectively and tested using QCA Designer Tool. By these basic layouts further complicated layouts can be designed with less number of cells and area comparatively. The operation of the structures has been verified according to the truth table. The design works efficiently and produces required results. The logical structures thus designed, may be used as a basic building block of a general purpose Nano processor which may be a future technical advancement of this work.

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