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# Bias Stability of a-IGZO TFT and a new Shift-Register Design Suitable for a-IGZO TFT

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***Abstract*—**We have fabricated a-IGZO TFT and investigated the stability under positive DC and AC bias stress. The threshold voltage of a-IGZO TFT shifts positively under those biases, and that reduces on-current. For this reason, conventional shift-register circuit employing TFTs which stressed by positive bias will be unstable, may do not work properly. We have designed a new 6-transistor shift-register, which has less transistors than prior circuits. The TFTs of the proposed shift-register are not suffering from positive DC or AC stress, mainly kept unbiased. Despite the compact design, the stable output signal was verified through the SPICE simulation even under RC delay of clock signal.

***Keywords*—**Indium Gallium Zinc Oxide (IGZO), Thin Film Transistor (TFT), shift-register

## I. Introduction

AMORPHOUS Indium-Gallium-Zinc-Oxide (a-IGZO) is a promising candidate for high performance TFT because it shows high field-effect mobility and on-current while has very low leakage current [1],[2] and also, can secure uniform TFT characteristics when fabricated in large area [3].

Some companies integrate shift-register, which generates gate-pulse signal, using amorphous silicon TFT (a-Si TFT) to reduce cost of driver ICs [4], [5]. Similar attempts were investigated by some researcher group to integrate shift-register using a-IGZO TFT instead of a-Si TFT [6], [7].

However, most shift-registers include transistor which gets clock signal (AC) or positive DC for gate input bias. Under that condition, the threshold voltage of TFT will be shifted positively, and the on-current will decrease [8]-[13], so that the TFT is not working properly as time passes.

In our research, we have fabricated a-IGZO TFT and investigated the stability under positive DC and AC bias stress. Likewise prior report, the threshold voltage shifted positively under those biases, and that caused reduction of on-current. In such a case, conventional shift-register circuit employing TFTs which stressed by positive bias will be unstable, may do not work properly. Therefore, we aimed to design shift-register circuit which is not suffering from positive DC or AC stress. This paper will show successful circuit design and simulation results that meet our goal.

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## II. a-IGZO TFT Fabrication and Charateristics

We fabricated the inverted-staggered etch stopper structure oxide-based TFTs. Gate metal (Mo) was deposited by DC sputtering on a glass substrate. SiO2 layer was deposited by plasma enhanced chemical vapor deposition (PECVD) for gate insulator and then active layer was deposited by sputtering. After active island patterning, etch-stopper layer was deposited and patterned to prevent back surface damage from post process. Source/drain electrodes (Mo) were deposited by sputtering and patterned. Finally, SiO2 layer was deposited for passivation. After fabrication finished, TFT was annealed at 300 ℃ in air condition. Figure 2 shows the schematic cross-section view of fabricated a-IGZO TFT.

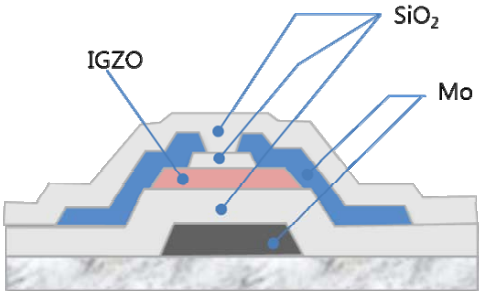



Fig. 1 Schematic image of fabricated a-IGZO TFT

We measured the TFT of which width/length ratio is 50um/10um. To analyze transfer characteristics with semiconductor analyzer (Agilent B1500A), the gate voltage was swept from -20 V to 20 V at 0.2V step and drain voltage was 10 V while source electrode was grounded.

The measured transfer curve is showed in Figure 2. The saturation mobility is 8.62cm$^2$/Vs and the threshold voltage is 0.67V. The steep sub-threshold slope (0.34V/decade) suggests that a-IGZO TFT has lower sub-gap state near conduction band edge (Ec) than a-Si TFT.

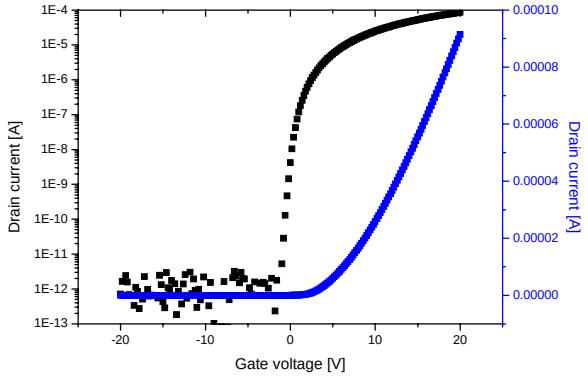



Fig. 2 Transfer curve of a-IGZO TFTs

To investigate bias stability of fabricated a-IGZO TFT, negative and positive bias was applied to the TFT, respectively. Negative bias condition is that gate to source voltage (Vgs) is -20V and drain to source voltage (Vds) is kept at 10V. The initial and final (after 10000 seconds) transfer characteristics are exhibited in figure 3. We can hardly see the differences in both curves. That is, a-IGZO TFT is stable under negative bias stress.

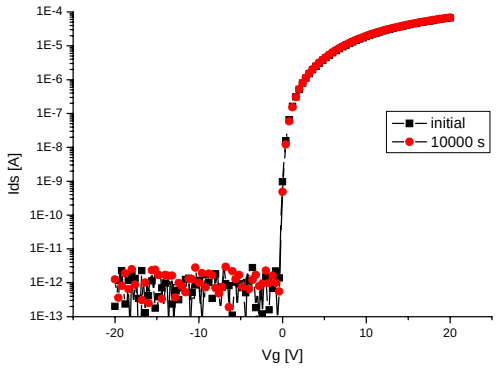
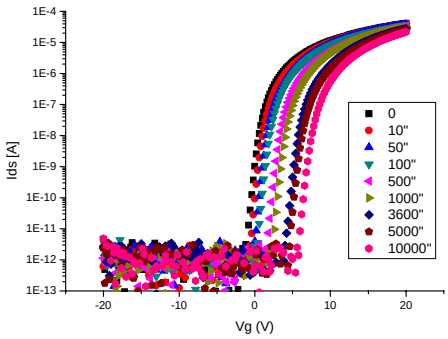
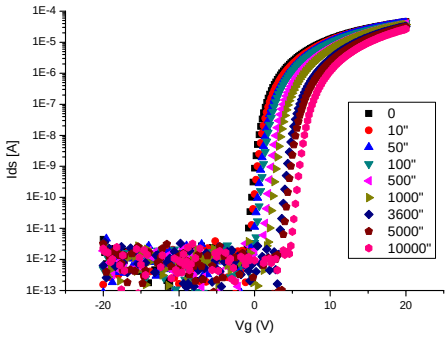



Fig. 3 Transfer curve shift under negative bias stress : Vgs=-20V, Vds=10V

To investigate the stability under positive bias stress, we tested electrical bias both DC and AC stress. Figure 2 (a) shows the transfer curve shift under positive DC stress at Vgs=Vgd=30V for 10000 seconds. Threshold voltage shift (Vth shift) is about 6V, a large value considering relatively short time. Figure 2 (b) shows the transfer curve shift under AC stress, which has 50% duty ratio, 20us pulse width and $V_{high}$=30V, $V_{low}$=0V. Vth shift under AC stress is about 5V, this value is a bit lower than that of DC stress but still large value. TFTs under these conditions will not work well in short period. These trends of Vth shift are agreement with previous reports [8]-[13]. Therefore, it is desirable to design circuit with TFTs which avoid suffering from positive DC or AC (=clock) for gate input bias.




(a)



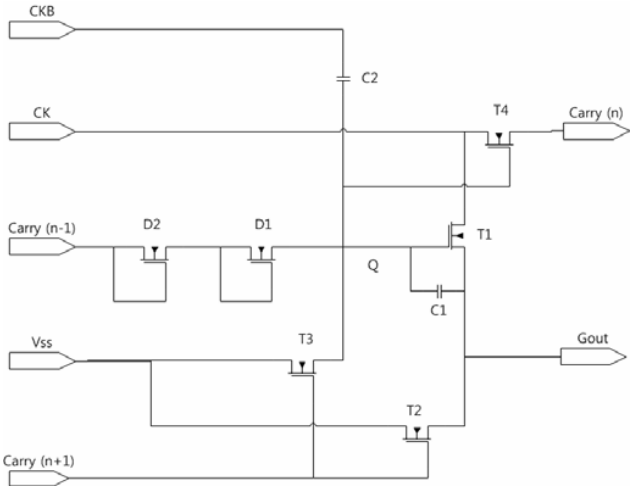

(b)

Fig. 4 Transfer curve shift under bias stress : (a) positive DC (Vgs=Vgd=30V), (b) positive AC (duty=50%, pulse with=20us, $V_{high}$=30V, $V_{low}$=0V, Vd=Vs=0V)

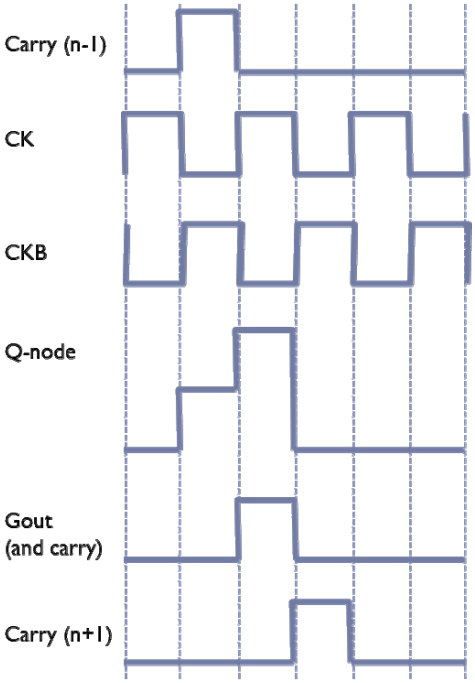
## III. Shift-register Design

We devised novel compact design of shift-register. Figure 3 (a) represents schematic design of our proposed shift-register and Figure 3 (b) exhibits schematic input/output signal. Carry signal from previous stage [carry (n-1)] enters Q-node through D2 and D1 diodes, and then Q-node is floated. CK signal varies from low state (Vss) to high state (Vdd). That makes current flow through T1, so that the potential of Gout and carry (n) will increase up to Vdd, also Q-node is boosted up to higher voltage by C1. When carry signal from next stage [carry (n+1)] enters into T2 gate and T3 gate, Gout and Q-node is reset to Vss, and then floated. We can verify there is none of transistors stressed by positive DC or AC (=clock).

As mentioned above, after turning-off of T3, Q-node is floated and coupled to CK due to parasitic capacitance between CK and T1. That makes Q-node potential unstable, in other words, a ripple voltage is generated by coupling to CK.




(a)




(b)

Fig. 5 Schemacic design of proposed Shift-register (a) and input/output signal (b)

The role of C2 is to stabilize or alter phase of Q-node ripple. C2 supplies opposite charges to Q-node by coupling to CKB. We can estimate theoretically the ripple voltage of Q-node as below,

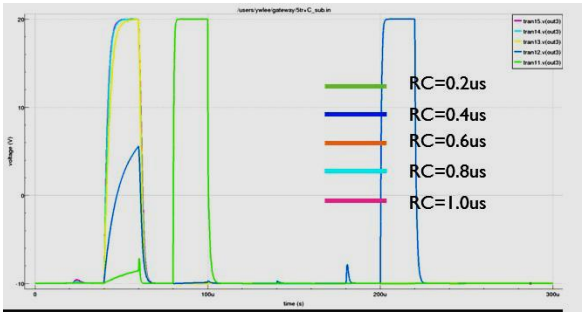
$$\Delta V = \frac{C_{parastic} - C_2}{C_{parastic} + C_2 + C_1} \times (Vdd - Vss)$$

Where, $C_{parastic}$ indicates the capacitance between CK and T1 and makes Q-node unstable.

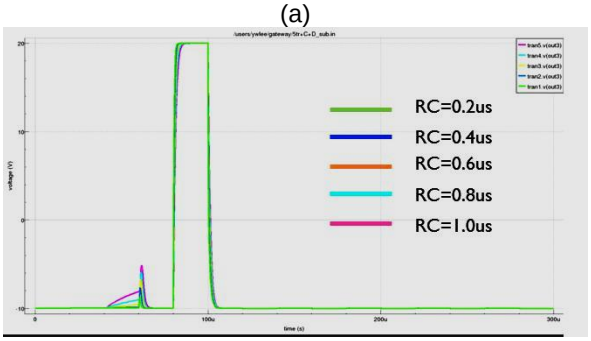
By above equation, we expect that if C2 is larger than $C_{parastic}$, we can convert the phase of Q-node ripple. Important meaning of converted phase of ripple is that when CK is high state, the ripple is low state, so that Vss potential of Gout is less affected by CK during hold time.

We simulated Gout by constructing cascade of shift-register, and show the results in Figure 4. We have verified that the larger clock delay is inputted, the worse Gout is produced. Therefore, it is desirable to consider RC delay of CK to verify reliability of circuit.

Figure 4 (a) shows the case of removing D2 diode from shift-register in Figure 3 (a). There are abnormal outputs except for 0.2us-RC. However, by employing D2, we can verify stable output in Figure 4 (b). Because D2 eliminates or lowers the carry noise, more stable carry signal can be inputted to D1.




(a)




(b)

Fig. 6 Simulation results of Gout :
(a) simulation w/o D2, (b) simulation w/ D2 diode (where, RC is time delay constant of clock signal)

## IV. Conclusion

We have fabricated a-IGZO TFT and investigated the stability under negative and positive bias, respectively. While a-IGZO TFT is stable under negative bias stress, it is severely shifted under positive DC/AC bias. Positive shift reduces the on-current, so that conventional shift-register circuit employing TFTs which stressed by positive bias will be unstable, may do not work properly. Therefore, we aimed to design shift-register circuit in which is no positive DC or AC stress. And we proposed a new 6-transistor shift-register, which has less transistors than prior circuits. The TFTs of the proposed shift-register are not suffering from positive DC or AC stress, mainly kept unbiased. Despite the compact design, the stable

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## ACKNOWLEDGMENT

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