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Study of Two Writing Schemes for a Magnetic Tunnel Junction Based On Spin Orbit Torque

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***Abstract*—**MRAM technology provides a combination of fast access time, non-volatility, data retention and endurance. While a growing interest is given to two-terminal Magnetic Tunnel Junctions (MTJ) based on Spin-Transfer Torque (STT) switching as the potential candidate for a universal memory, its reliability is dramatically decreased because of the common writing/reading path. Three-terminal MTJ based on Spin-Orbit Torque (SOT) approach revitalizes the hope of an ideal MRAM. It can overcome the reliability barrier encountered in current two-terminal MTJs by separating the reading and the writing path. In this paper, we study two possible writing schemes for the SOT-MTJ device based on recently fabricated samples. While the first is based on precessional switching, the second requires the presence of permanent magnetic field. Based on an accurate Verilog-A model, we simulate the two writing techniques and we highlight advantages and drawbacks of each one. Using the second technique, pioneering logic circuits based on the three-terminal architecture of the SOT-MTJ described in this work are under development with preliminary attractive results.

***Keywords*—**Spin orbit Torque, Magnetic Tunnel Junction, MRAM, Spintronic, Circuit simulation.

I. Introduction

A variety of random access memories (RAMs) exist in the current semiconductor market. Each of which has its own qualities and shortcomings. Dynamic RAM (DRAM) offers high density, Static RAM (SRAM) is rapid and robust and Flash RAM ensures the Non-Volatility (NV) feature. Thinking the end was near for CMOS technology scaling, the ITRS declared a prompt need for a new replacement technology, especially with the increase of the static power due to the leakage current in sub-90nm CMOS integrated circuits (ICs). A number of companies entered the race for innovative technologies toward a "universal memory" which could replace all conventional memory types while gathering their most merits; speed, high density, cost benefits, endurance and Non-Volatility.

Among the possible scenarios in the future, the magnetic tunnel junction (MTJ) [1] is one of the most relevant candidates. In addition to non-volatility merit, the resistance value property (several kΩ) makes the magnetic technology compatible with CMOS process which is a key feature for emerging technologies. The first commercial MTJ based MRAM was produced successfully in 2006 [2]. Several semiconductor companies (IBM, Samsung, Toshiba, NEC, TSMC…) have published results on operational MRAM test chips and announced MRAM products [3]. Emerging MRAM technologies have begun with Field-Induced Magnetic Switched (FIMS) [4] MRAMs that have been in product for several years now. Then, the selectivity was improved by the so-called "toggle" approach proposed in [5], but field-based writing schemes remain hardly scalable below 90nm. Then, Crocus Technology developed the Thermally Assisted Switching (TAS), which allowed solving the selectivity issues while reducing the writing energy and improve the scalability [6]. Both consist of a Magnetic Tunneling Junction (MTJ) as a storage element and require high writing current and consequently increased power consumption and die area due to large transistors and huge write lines. Also magnetic-field-based MTJs suffer from the lack of robustness against downscaling. Now, more advanced writing scheme, known as "Spin Transfer Torque (STT)", is under development to solve the latter issues. Spin polarized current can be used through the junction to apply Spin Transfer Torque (STT) [7], [8] http://www.hindawi.com/journals/ijrc/2008/723950/ - B9 and switch the magnetization of the storage layer, without requiring an external magnetic field.

STT device has succeeded to reduce the writing current and improve the scalability over the FIMS MRAM generations. However, two main shortcomings are still limiting the reliability and endurance of STT-MRAMs; i) The high current density required for writing can occasionally damage the MTJ barrier, ii) It remains a challenge to fulfill a reliable reading without ever causing switching, Since writing and reading operations share the same path (through the junction). In some recent works [9]-[11], a number of STT-MRAM with three-terminal architecture were proposed to overcome the latter issues. But, the reliability has been improved at the cost of the switching time, the required area and the complexity of the fabrication process (additional materials and layers).

In this paper, we deal with an exotic three terminal MRAM based on a concept of switching known as "Spin Orbit Torque (SOT)" [12], also called spin-orbit-coupling or spin-orbit interactions. Thanks to its three-terminal architecture, authors in [13]-[15] claim that Spin-Orbit-Torque (SOT) switching devices can be build with independent reading and writing paths and so avoid challenges encountered with the current state of the art of conventional STT-MRAMS, while keeping competitive switching currents.

For the design of "hybrid CMOS" Integrated circuits (ICs) including this emerging technology, it becomes a fundamental

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step to define a compact model of the SOT-MRAM. To the best of our knowledge, this work represents the first simulation results describing two writing schemes of the SOT-MTJ based on a macro-model written in Verilog-A. The most significant physical phenomena responsible for the SOT-MTJ behavior are taken into account and realistic parameters are used thanks to a close interaction with our laboratory technologists working on the characterization of the SOT device.

The paper is organized as follows: In section II, we present the SOT-MTJ device as well as a brief description of the model. Then, in Section III, we explore two possible writing schemes to switch the device magnetization. Section IV is the discussion. Finally we conclude the paper in Section V.

II. Spin Orbit Torque Based MTJ (SOT-MTJ)

Magnetic Tunnel Junctions are used as the basic memory elements in MRAM cells and magnetic logic devices. The MTJ is a nanostructure composed of two ferromagnetic layers (FM) (e.g. CoFeB) separated by a thin layer of insulator (e.g. MgO) which represents the tunnel barrier. The first FM layer (hard layer) -with a pinned magnetization- acts as a reference while the second FM layer (soft layer) -with a free magnetization- acts as a storage layer.

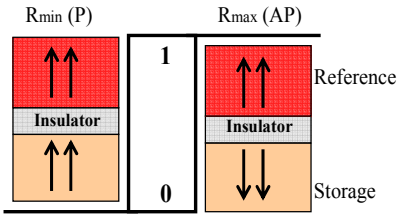


Fig. 1 Resistance variation of the MTJ according to the storage layer magnetization state

The magnetization of the storage layer can be switched between two stable states, either parallel (P) or antiparallel (AP) with respect to the reference layer. Electrons can tunnel through the thin barrier (~1nm) when a bias voltage is applied between the two electrodes of the device. The MTJ resistance is low (or high) for a P (or AP) magnetization configuration. These two configurations can be used to code two different logic states; logical 0 and 1, for instance (Fig. 1).

A. SOT-MTJ Structure

Reading and writing through the MTJ represents the weakness of traditional STT devices. STT-MTJ based technology has the following critical shortcomings for compatibility with future scaled CMOS technologies.

- The high drive current needs a large access transistor leading to an increased area.
- The current conduction through the tunnel junctions decreases reliability because of the high voltage. (i.e., the high current density required for writing can occasionally damage the MTJ barrier)
- Since writing and reading operations share the same path (through the junction), it remains a challenge to fulfill a reliable reading without ever causing switching.

For these reasons, it is of great interest to pursue exploring technologies for MTJ based MRAMs which provide a better reliability. Thanks to its three-terminal architecture, authors in [13], [15] assert that Spin-Orbit-Torque (SOT) switching devices can be build with independent reading and writing paths and so increase the reliability feature. An exciting controversy is in progress between research groups inquiring about the exact origins of the SOT switching mechanism. It is still not clear whether the Rashba effect has the dominant role to achieve the switching [12], [13] or it is only due to the Spin Hall Effect (SHE) [14]-[16]. That's why; we name this innovative device as "SOT-MTJ", since this term reveals the spin-orbit-torque responsible for switching independently from its origin whether it is Rashba effect, SHE or both phenomena. However, in some papers [14]-[16], authors call the SOT MRAM as "Giant Spin Hall Effect (GSHE)" MRAM, believing that the spin-orbit-coupling is only due to the SHE occurrence.

A representative geometry of a 3-terminal memory cell with the perpendicular switching of the magnetized ferromagnetic layer using the SOT writing mechanism is shown in Fig. 2. The structure consists of a free layer nanomagnet on the top of a conductor (metal electrode). For clarity reasons, we present only the main layers of the MTJ stack. Additional layers and materials combination could be considered to increase the robustness of the whole structure and retrieve undesirable effects (e.g. dipole fields around the free layers, etc). For instance, a more complex and complete structure has been proposed in [16]. The writing electrode materials existing in literature to fabricate the sample device are: β-Tantalum (β-Ta), β-Tungsten (β-W) or Pt [13]-[15]. The magnetic cell is written by applying a charge current via the write line. The orientation of the storage layer magnetization is controlled by the direction of the applied charge current. Positive currents (along +x) produce a spin injection current with transport direction (along +z) and spins pointing to (+y) direction. The injected spin current in-turn produces spin torque to align the magnet in the +y or –y direction.

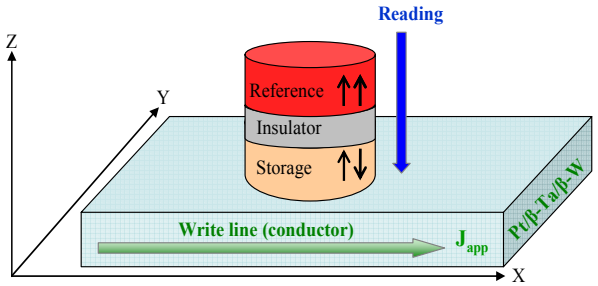


Fig. 2 Schematic of the three-terminal SOT device and the two independent paths for read and write operations. In-plane current injection through the write line (conductor) induces the perpendicular switching of the storage layer

B. SOT-MTJ Modeling

In order to simulate the switching behavior of the SOT-MTJ, we developed a compact model written in Verilog-A. Our choice of the coding language was motivated by the capability of Verilog-A to afford a quick method of enhancing compact models to illustrate new physics of advanced processes. In addition, it is on the path to becoming the preferred compact modeling language for both academic and industrial research groups. The modeling approach used for the SOT device is detailed in [17]. It proves efficiency and describes straightforward, high-speed and precise electrical representation of the physical behavior of the SOT-MTJ device. In order to develop this model, we proceed under the macrospin approximation. We consider that the magnetization of each ferromagnetic layer is uniform (single domain). Then, we analyze the model equations along with some approximations. Finally, thanks to close exchanges with Spintec technologists -working on the fabrication and characterization of the SOT-MTJ- a number of associated parameters are fed into these equations. The model describes the memory cell as a three-terminal logic device and includes the dynamic behavior described by the Landau–Lifshitz–Gilbert model (LLG) [18]. To follow the variation of the SOT-MTJ resistance, Julière's model [19] as well as Simmons's model [20] is used in the expression describing the conductance through the junction. Moreover, for an improved accuracy, we integrate the dynamic conductance given by Brinkman model [21] and we take into consideration the dependence of magneto-resistance on bias voltage. Finally, a special interest is given to Rashba effect and SHE torques inside the LLG equation to highlight the impact of these two factors on the dynamic of magnetization switching intensively argued in [12]-[16].

III. SOT-MTJ Switching Schemes

This section describes two different switching schemes. While the first does not need an external magnetic field to switch the device magnetization, the second requires a permanent magnetic field. Each method has its advantages and drawbacks that we detail in this part of work. All simulation results shown in this part are run with Spectre simulator under Cadence Virtuoso platform.

A. Switching during Precession Dynamics

Back et al were the first who made evidence of this mode of switching [22]. If we use the suitable value of the writing current and the appropriate pulse width, it is possible to apply this approach of switching in the case of the SOT-MTJ device.

1. Simulation Results

The initial magnetization of the soft layer of the SOT-MTJ is along the z axis in the positive direction of the Cartesian coordinates. In all simulation figures, the perpendicular magnetization is abbreviated as "m_z". During the applied current period, the magnetization becomes in the plane (x, y). But before attaining a stable state, it shows a precessional behavior (the damping effects also is taken into consideration in our model since it is included in the LLG equation [18]).The magnetization along the z axis oscillates according to a pseudo-periodic regime as shown in Fig. 3. At this point, it is important to control the pulse width in order to achieve only a half period of precession. Depending on the sign of the half period (+z or –z), the magnetization is released into the up state (+z) or the down state (-z).

In Figs. 3 and 4, we illustrate the principle of precessional switching and we highlight its direct dependence on the applied current density and the pulse width.

At first, we study the impact of the applied current on the switching mechanism. The experiments results delivered by research teams working on SOT devices [12]-[16] claimed that the current density threshold required for switching the magnetization from P (AP) to AP (P) has the same value (symmetrical switching). It is of the order of $J_{app}=10^{12}A.m^{-2}$. Thus, we observe the perpendicular magnetization m_z for different values of J_{app} starting from $J_{app}=1x10^{12}A.m^{-2}$.

Fig. 3 shows that at J_{app} = (1-2) $x10^{12}A.m^{-2}$, the spin torque is not enough to act on the magnetization of the storage layer, the initial state (m_z=1) does not change during the pulse and no oscillations are observed. Starting from a value of $J_{app}=3x10^{12}A.m^{-2}$, we can notice the manifestation of a spin torque action on the magnetization: the oscillating behavior appears till attaining the stability. For higher current density J_{app}, the precession appears earlier and the pseudo-period is smaller.

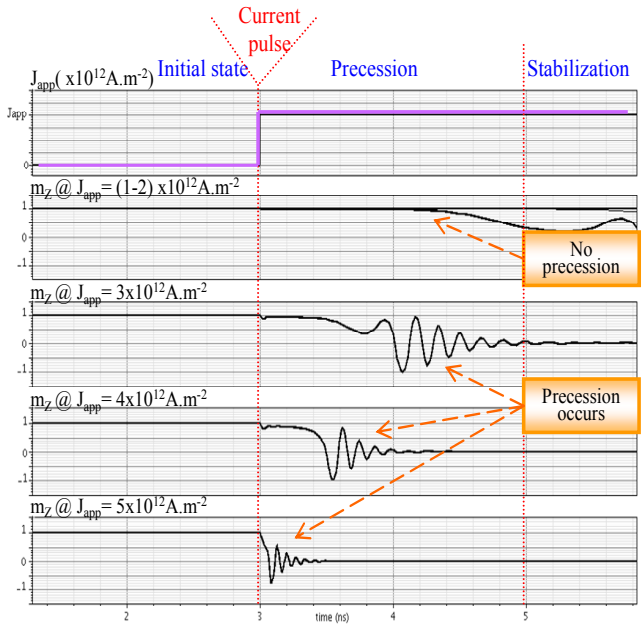
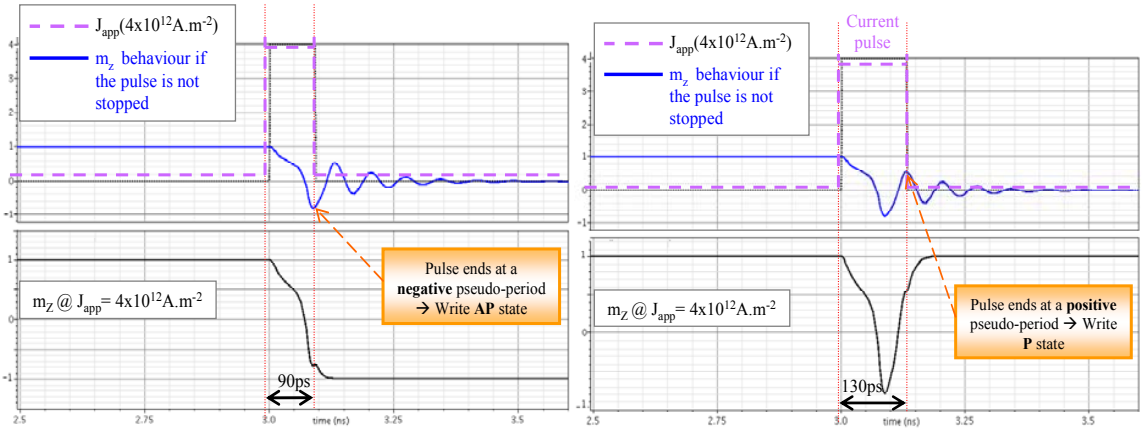


Fig. 3 Study of the dynamic behavior of the perpendicular magnetization m_z according to the variation of the current density J_{app}

Fig. 4 describes the precessional technique to write a SOT junction. We choose a study case of $J_{app}=4x10^{12}A.m^{-2}$. Thus the pulse width of the writing current is 90ps and 130ps to write the AP and the P states, respectively. If we write with a lower current, larger pulses are required and vice versa.

The pulse width of the applied current controls the switching of the magnetization m_z:

- If the pulse ends at a negative pseudo-period, as shown in Fig. 4 (a), the MTJ is configured to the AP state.
- If the pulse ends at a positive value of the pseudo-period, as shown in Fig. 4 (b), the MTJ is configured to the AP state.



a) Write of the AP state with a 90 ps pulse width b) Write of the P state with a 130 ps pulse width

Fig. 4 Writing process of the Parallel (m_z=1) and Anti-Parallel (m_z=-1) states

2. Benefits and Limitations

The approach of precessional writing gives the possibility to reverse the magnetization of the soft layer with an extremely high speed. Only a very short pulse of writing current is required. This mode of writing achieves speeds of the order of a few hundred picoseconds and can even reach smaller values if we write with a higher current. Although the approach seems interesting and allows high speed switching, it requires extremely precise writing pulses. This fact limits the feasibility of precessional writing to implement high density memory architectures. By using a smaller current, we can increase the pulse width required for writing, since larger pseudo-periods are obtained during precession (Fig. 3). This can also decrease the power consumption during writing since a smaller current is used.

In the next section, we describe a second technique of writing the SOT-MTJ which is more realistic and which has been already validated by fabricated devices [13], [15].

C. Switching in the Presence of an External Permanent Magnetic Field

In fact, during the time of the applied current pulse, the magnetization vector m_z oscillates at first till stabilizing at the zero value. If the pulse is short and ends during precession, we showed that the reversal of the m_z magnetization is possible (Fig. 4). But, it requires very short and sharp pulses.

If a large pulse is applied -which ends after the precession time-, the m_z magnetization has an identical probability to be oriented up or down along the z-axis. If there is no external applied field H_a, an arbitrary switching occurs that may be caused by nucleation events [13]. The solution used by research teams working on the realization of the SOT device [13], [15], is the generation of a permanent magnetic field B_a by adding a permanent magnet on chip or a biasing layer on top of MTJs. The field H_a contributes to the control of switching when a pulse of writing current is applied. Fig. 5 illustrates the behaviour of the SOT-MTJ in the presence of a permanent magnetic field: Starting from the initial magnetization, the AP or the P states are obtained by applying a negative current pulse or a positive current pulse, respectively. In Fig. 5, the permanent magnetic field is negative (B_a<0). It is also possible to work with a positive B_a (B_a>0). But the effect of the current pulses will be simply inverted, as explained in the pseudo code in Fig. 5 (c). More details about the switching mechanism are available in [13]-[16].

Fig. 6 shows the simulation results of m_z reversal according to the current pulse in the presence of a negative field (B_a<0). If a negative pulse is applied, the magnetization is reversed downward (m_z=-1) while a positive pulse switches the magnetization upward (m_z=1).

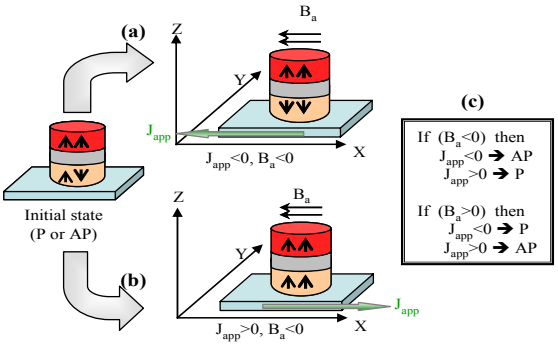


Fig. 5 Switching dependence on the applied field and current directions

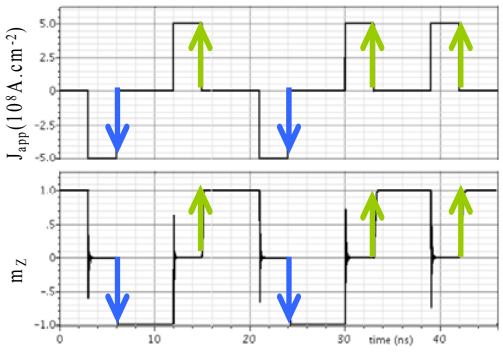


Fig. 6 Simulation of the dynamic behavior of the perpendicular magnetization m_z according to the current

IV. Discussion: Limitations, Advantages and Future of the SOT-MTJ

Based on the simulation results which are in accord with the first experimental characterizations of SOT-MTJs available in literature [13], [15], we described and simulated two writing schemes of this innovative junction. The first scheme does not require any external magnetic field, which means that no additional bias layer is required for the fabrication process. High speed of writing can be achieved. However, the approach can suffer from synchronization issues for the design of memories architectures because of the difficulty to generate very accurate and sharp writing pulses (in the order of hundreds of picoseconds). A small variation of the time to rise/fall of the pulse can skew the writing. The second writing scheme requires an external permanent field. This technique is experimentally demonstrated in [13], [15] and the characterization of the fabricated samples have revealed very hopeful results. The external magnetic field can be generated simply by adding a bias layer or a magnet on top of the whole chip. So, it is not expected to be a crucial issue.

It is worth to point out that the first fabricated devices show a high current density required for the magnetization switching (J_{app}~2-3 x10^{12}A.m^{-2}) and consequently a high writing current (>2mA). However, researchers working on the SOT concept are optimistic about the future of this device and claim that the current can be decreased with further interface engineering. In [13], [15] authors claimed that shrinking the width of the writing microstrip to be equal to the dimension of the long axis of the nanopillar or, further reducing the demagnetization field of the FM free layer [23], [24], the required current for SOT devices could be reduced to <100µA. At such a current value, three-terminal SOT devices would be very competitive with the efficiency of conventional STT-MTJs [25], [26]. Three-terminal SOT approach can even overstep the two-terminal STT devices since it separates the reading and the writing paths. This enhances the reliability of devices and overcomes the main challenges encountering MRAMs.

In [16] an interesting predictive study of the SOT-MTJ device has been conducted by researchers in Intel. It showed that this inventive MRAM can enable better energy- delay and voltage performance than traditional MTJ based STT devices at scaled nanomagnet dimensions (10-30nm). Optimized SOT devices can enable MRAM with scaled nanomagnets (30nm X 60nm), ultra-low voltage operation (< 0.1 V), fast switching times (10 ps) and switching energy as low as 100 aJ/bit.

Although it is still in its infancy, the three-terminal architecture of SOT devices promises efficiency and easiness for the fabrication process.

V. Conclusion

This paper presents a study of two possible writing schemes for a three-terminal MTJ nanopillar based on the SOT approach. Thanks to an accurate Verilog-A compact model, we could observe the switching behavior of the SOT-MTJ according to two different writing techniques. While precessional switching allows very high speed, its feasibility is limited by the very small pulse width required for writing. The second technique, already validated in research laboratories by fabricated samples, requires an external magnetic field and offers straightforward fabrication process. By using the latter writing scheme, a number of hybrid MTJ/CMOS logic circuits are under examination in our laboratory with inventive architectures thanks to the three-terminal structure of the SOT-MTJ.

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