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Off-State Leakage Power Reduction by Automatic Monitoring and Control System

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***Abstract*—**This paper propose a new circuit design which monitor total leakage current during standby mode and generates the optimal reverse body bias voltage, by using the adaptive body bias (ABB) technique to compensate die-to-die parameter variations. Design details of power monitor are examined using simulation framework in 65nm and 32nm BTPM model CMOS process. Experimental results show the overhead of proposed circuit in terms of its power consumption is about 10 μW for 32nm technology and about 12 μW for 65nm technology at the same power supply voltage as the core power supply. Moreover the results show that our proposed circuit design is not far sensitive to the temperature variations and also process variations. Besides, uses the simple blocks which offer good sensitivity, high speed, the continuously feedback loop.

***Keywords*—**leakage current, leakage power monitor, body biasing, low power

I. Introduction

TECHNOLOGY scaling of MOSFET into sub-100 nm region has resulted in significant increase in leakage power consumption, due to reduction in threshold voltage, channel length and gate oxide thickness [2]. The process variations can be classified as die-to-die (inter-die) variations or within-die (intra-die) variations. In die-to-die variations, all devices on the same die are assumed to have the same parameters. However, devices on the same die are assumed to behave differently for within-die variations [9].

In nanoscaled CMOS devices, there are many leakage sources such as gate leakage, subthreshold leakage, BTBT-based leakage, GIDL, DIBL, etc., the total leakage current in the off state n-MOSFET is given by [3]:

$$I_{leakage} = I_{SUB} + I_{BTBT} + I_{GIDL} + I_{GB} + I_{DG}$$

We briefly describe some important type of leakage current in this section.

-Gate Induced Drain Leakage (I_{GIDL}): I_{GIDL} is a current from the drain to the substrate caused by the high electric field between the gate and the drain; thin gate-oxide thickness and a high supply voltage increase GIDL [13].

-Band to Band Tunneling Leakage (I_{BTBT}): In a high electric field (greater than 10^6 volts per centimeter), electrons tunnel across the reverse-biased PN junction of drain and source substrates, in what is known as junction BTBT [13]. I_{BTBT} increases exponentially due to increased size of lightly doped drain region.

-Gate Oxide Tunneling Current (I_G): Reduction of gate oxide thickness results in an increase in the field across the oxide. The high electric field coupled with low oxide thickness results in tunneling of electrons from substrate to gate and also from gate to substrate through the gate oxide, resulting in the gate oxide tunnelling current [15].

-Subthreshold Leakage (I_{SUB}): Subthreshold or weak inversion conduction current between source and drain in an MOS transistor occurs when gate voltage is below V_{TH}. Subthreshold Leakage is exponentially related to V_{TH} [15].

In terms of magnitude, the most important sources of leakage are: gate oxide tunneling based leakage (~54.79%), subthreshold leakage (~44.5%), and Band-to-Band-Tunneling based leakage (~0.68%) for 45 nm Bulk-CMOS. Other components of leakage include Gate Induced Drain Leakage (GIDL), Drain Induced Barrier Lowering (DIBL), etc. The magnitude of each leakage component depends on the process technology used. Use of high-K dielectric gate helps reduce gate oxide leakage current. However, when high-K dielectric is used, the channel mobility degrades leading to reduced performance [5]. The high dielectric constant with the same gate capacitance allows a larger physical thickness to suppress the edge direct tunneling. However, high-k insulators introduce subtle capacitive coupling phenomena known as FIBL that can lead to poor short channel performance which makes the decreased I_{OFF} increase [11].

II. Background and Related Work

Leakage reduction techniques can be characterized into two classes: runtime techniques and design-time techniques [2]. To minimize leakage power dissipation, researchers have proposed several circuit techniques such as multi threshold-voltage CMOS (MTCMOS) and variable threshold-voltage CMOS (VTCMOS) using variable substrate bias voltage. Another technique with little or no overhead is the input pattern control technique based on the stack effect [13].

Reverse Body Biasing (RBB) has widely been used to reduce the leakage power of devices. However, most recent research has shown that if RBB is too high, leakage power can actually increase due to the contribution of the Band-to-Band Tunneling currents. To prevent this problem a new optimal body biasing system is required to balance the sub-threshold leakage with the BTBT leakage [7].

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References [3] and [7] introduce a leakage monitoring circuit, by using the concept of Reverse Body Biasing (RBB). These circuits compare extracted sub threshold leakage current (I_{SUB}) component with Band-to-Band Tunneling leakage current (I_{BTBT}) component simultaneously, then the optimal body bias is adjusted according to the temperature variations in the proposed approach. Reference [8] presents a more complete leakage monitoring circuit novel design method to minimize the leakage power during standby mode using a novel adaptive supply voltage and body-bias voltage generating technique for nanoscale VLSI systems. The process, voltage, and temperature (PVT) variations are monitored and controlled. The other important types of leakage monitoring circuits are briefly described as bellow:

Reference [12] proposed method to reduce the leakage current in nanometer CMOS circuits. The system consists of five stages; Leakage Monitoring Circuit, Voltage Controlled Oscillator (VCO), Phase Detector, Decoder, and Digital-to-Analog Converter. The separated leakage components (I_{SUB} and I_{BTBT}) are applied to the voltage controlled oscillator (VCO) to generate pulse waveforms proportional to the magnitude of each leakage.

References [1] and [4] present an in-situ (direct) power monitoring scheme using the voltage drop across the sleep transistor acting as a power sensor. The power monitor measures power directly from a given load circuit operating in active mode. Reference [10] discuses a leakage current monitor circuit for optimal body-biasing control which contains a symmetric pair of off-NMOS clusters. The proposed circuit determines V_{BODY} without absolute leakage measurement.

III. Proposed Leakage Power Monitor and Control Design

To reduce the standby leakage power, this paper proposes a new circuit design which determines the optimal reverse body bias voltage, by using the adaptive body bias (ABB) technique to compensate die-to-die parameter variations.

For standby mode leakage minimization depends on the particular technology employed and is sensitive to process variations. Furthermore, applying body bias reduces the impact of die-to-die and within die parameter variations. Thus, applying the optimal body bias leads to both minimum leakage current and improved yield [16]-[17].

Our new design technique automatically generates the optimal body bias voltage during standby mode, by monitoring the total leakage current ($I_{leakage}$) and comparing the value of $I_{leakage}$ at the time of t0 and t1 (t1 > t0). This system increases V_{TH} by adjusting body voltage in the RBB direction, so reduces total leakage current.

The proposed circuit is an in-situ (direct) power monitoring scheme using the current mirror circuit, which acting as a total leakage current sensor. The leakage current monitor measures total leakage current directly from a given load circuit, therefor the process, voltage, and temperature (PVT) variations are monitored and controlled, without any extra monitor and control circuits. Reference [8] is mentioned PVT variations but it is used the circuit with the high overhead to control PVT variations.

The proposed scheme in Fig. 1 consists of a total leakage current monitor circuit, comparator and quantizer, and the body voltage generator. The total leakage monitor circuit is used to monitor the leakage current during standby mode directly from a given load circuit. Fig. 2 shows expanded power leakage ($P_{leakage}$) monitor circuit with feedback loop, a key component of the V_{BODY} controller. Leakage monitor circuit itself consist of two separate current mirror circuit, where the transistors M1, M2 and M3 are the replica transistors to sample total leakage current. Fig. 3 shows a timing chart of the $P_{leakage}$ monitor circuit, transistors M4 and M5 was controlled with signals S.a and S.b.

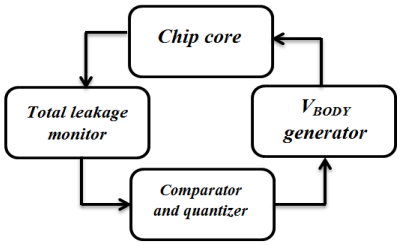


Fig. 1 Block diagram of the proposed V_{BODY} control system

Here we explain the functionality of proposed circuit, with an example for better clarity. Fig. 4 illustrates the curve that should be scan by $P_{leakage}$ monitor circuit, to find the optimum body bias voltage, Assume that minimum leakage current occur at point P5, the power monitor operates in three phases. First, when signal S.a is high, so M4 is on and leakage current, sampled and replicated to M2, this sampled current charges C1 capacitor, and will be held until next measurement cycle. Second phase, when signal S.b is high, during this operation M5 is on and leakage current, sampled and replicated to M3. Finally timing control signals turn off M4 and M5, then the value of VC_1 and VC_2 inject to sense amplifier block. This block offers good sensitivity, high speed, and low-power dissipation. The leakage current at point P2 is smaller than point p1, so $VC_2<VC_1$, and signal O5 order to reverse the body bias voltage more. Table I summarizes outputs of the main node in the circuit for each states which leakage power monitor encounters for this example.

The key signal in this circuit is O5, which order the V_{BODY} generator block to forward or reverse the body bias voltage. In fact there are four modes of operation of this circuit.

1) If $VC_1 > VC_2$ (O1=1) and O3 = 0, then O5=0 and V_{BODY} goes to reverse direction.

2) If $VC_1 < VC_2$ (O1=0) and O3 = 1, then O5=0 and V_{BODY} goes to reverse direction.

3) If $VC_1 < VC_2$ (O1=0) and O3 = 0, then O5=1 and V_{BODY} goes to forward direction.

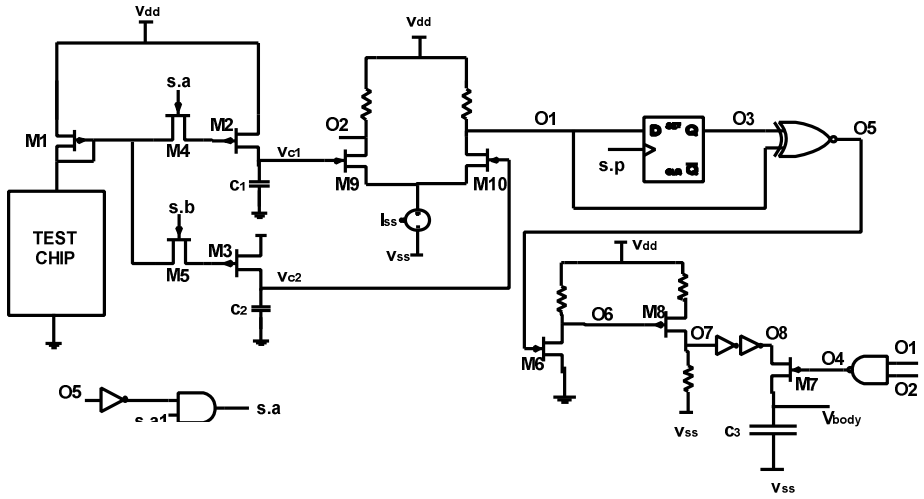


Fig. 2 Schematic of the proposed V_{BODY} control system

4) If $VC_1 = VC_2$, then O1=O2, and O4 = 0, maintaining the body-bias voltage.

D flip flop helps to have $O1_{t=t1}$ and $O1_{t=t0}$ ($O1_{t=t0}$ = O3) contemporaneous, when S.p changes from 0 to 1, $O1_{t=t0}$ fed to D flip flop, to over write on O3. Therefor the inputs of XNOR gate will be ready, to generate O5. The body bias voltages for transistors are automatically set by the control system to ensure that the chip dissipates minimal power in standby mode. The proposed scheme uses the simple blocks which offer the advantages, such as good sensitivity, high speed, the feedback loop continuously works and the most important ones low-power dissipation.

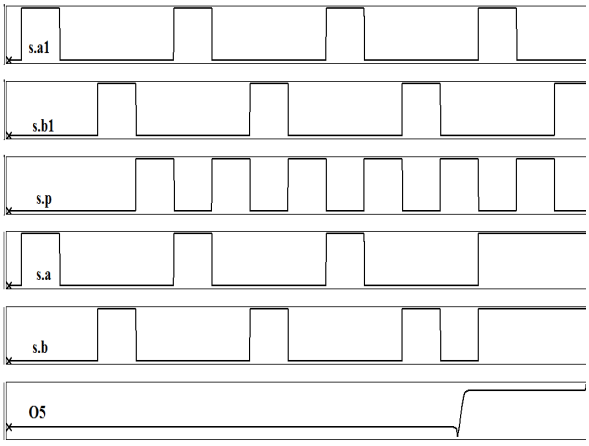


Fig. 3 Control signals for power monitor

This power monitor and control circuit automatically adjusts this V_{BODY} value, according to the process variations of the devices, to apply the optimal body bias. This body bias improves the nominal and worst-case total leakage caused by the process variations and is applicable to different technology generations. Thus proper monitoring of the total leakage results in lower leakage currents and higher yields.

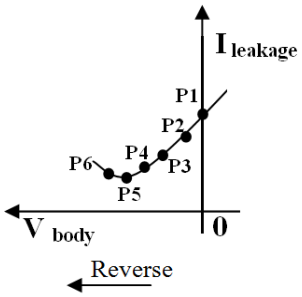


Fig. 4 Leakage states which activating by leakage monitor circuit

TABLE I
OUTPUTS OF THE MAIN NODE IN THE CIRCUIT FOR EACH STATES

$s.b_1$	s.a	s.b	V_{c1}	V_{c2}	O_1	O_2	O_3	O_4	O_5	v_{body}
H	L	H	P1	P2	H	L	L	H	L	Reverse
L	H	L	P3	P2	L	H	H	H	L	Reverse
H	L	H	P3	P4	H	L	L	H	L	Reverse
L	H	L	P5	P4	L	H	H	H	L	Reverse
H	L	H	P5	P6	L	H	L	H	H	Forward
L	H	H	P5	P5	H	H	L	L	×	Hold

IV. EXPERIMENTAL RESULTS

In this paper we propose a simple circuit to determine the optimal off-state body bias which has the minimum overhead

TABLE II
THE RESULTS FOR THE PROPOSED APPROACH AT 32NM TECHNOLOGY AND A TYPICAL CORNER

Circuit	# of gates	Function	leakage power (32nm)						% leakage power reduction (32nm)		
			Non optimized (uw)			Optimized (nw)					
			T=25°c	T=50°c	T=100°c	T=25° c	T=50° c	T=100°c	T=25°c	T=50°c	T=100°c
C432	160	27-channel interrupt controller	7.707	12.09	16.60	107.6	109.8	117.4	98.7%	99.09 %	99.2%
C499	202	32- bit SEC circuit	15.19	23.31	34.39	128.5	131.2	140.7	99.15%	99.4%	99.59%
C1355	546	32- bit SEC circuit	20.81	31.32	41.59	170.7	173.8	183.5	99.18%	99.44 %	99.55%
C1908	880	16- bit SEC/DED circuit	22.50	27.88	37.38	312.6	320.1	345.9	98.61%	98.85	99.07%

to compare with the other present circuits. We used Berkeley Predictive Technology process models (BPTM) to perform all experiments for 65nm and 32nm BPTM technology nodes. For the technology bellow 90nm the ITRS road map predicts that leakage power easily wins over dynamic power. Therefore, it is important to have efficient and accurate estimation of total leakage currents from all sources.

Simulation results in this paper, for proposed circuit and also benchmark circuits has been implemented in HSPICE for 65nm and 32nm BTPM model.

Our monitor power leakage circuit has been implemented and evaluated using ISCAS'85 benchmark circuits designed in the both technologies. Overhead of proposed circuit in terms of its power consumption is about 10 μW for 32nm technology and about 12 μW for 65nm technology at the same power supply voltage as the core power supply. This power dissipation is very small compared with the power consumption of the general digital cores.

The proposed system increases V_{TH} by adjusting body voltage in the RBB direction so as to reduce total leakage current. When the optimum body bias is detected, the body voltage adjustments are stopped to avoid excessive reverse body bias.

Table II shows the summary of the results for the proposed approach at 32nm technology and a typical corner (TT). The average leakage power has been measured using random input test vectors at 0.9 V supply voltage. Our leakage power monitor circuit has the capability to work accuracy at 65nm technology as well as 32nm; Table III indicates the simulation results of the benchmark circuits at 65nm technology and a typical corner (TT), by using random input test vectors at 1 V supply voltage.

As shown in the last partition of Table II and Table III, our new design for the minimal standby leakage power provides 98.6% up to 99.6% reduction in leakage power compared to the cases where any leakage reduction techniques are not used at all, for the same benchmark circuits. In order to show the efficiency of the proposed methodology for temperature the ISCAS'85 benchmark circuits are simulated at three temperature conditions (25^0 C, 50^0 C, and 100^0 C).

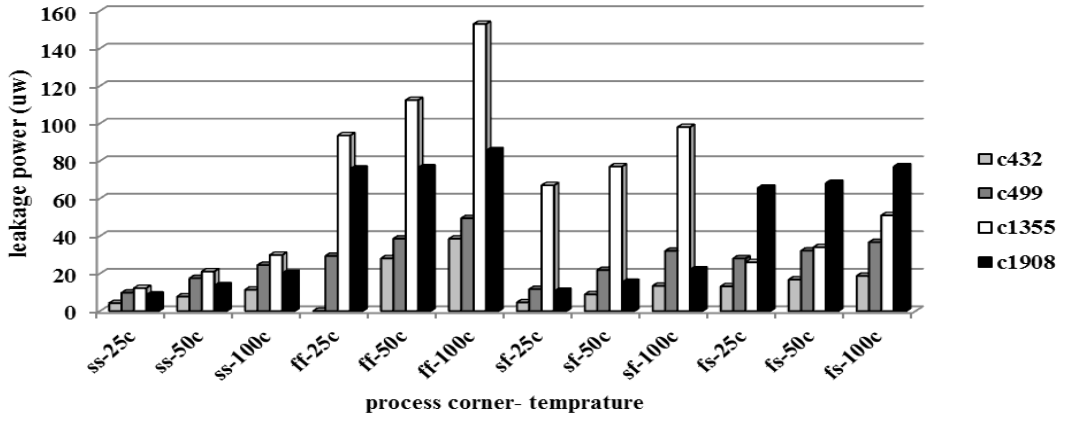
The results show that when the proposed technique is applied, the leakage power dissipation is not far sensitive to the temperature variations; because the circuit is an in-situ (direct) power monitoring scheme and optimal body bias voltage are changed adaptively according to the new temperature.

Process variations are gaining an increasing importance with the ever scaling technologies, as they directly affect leakage current, power performance and system reliability [6]. It is observed that as the supply voltage is reduced, the sensitivity of the circuit parameters to the process variation increases [14].

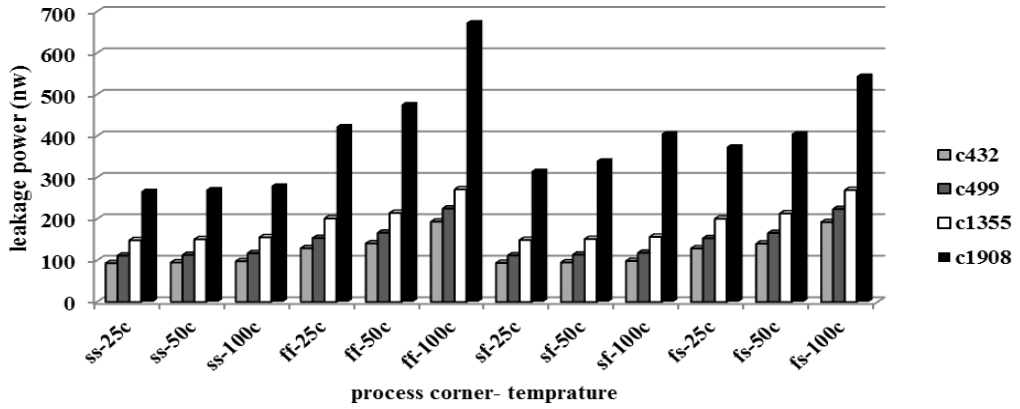
The most important process parameters considered are as follows: (1) T_{oxn}: NMOS gate oxide thickness (nm), (2) T_{oxp}: PMOS gate oxide thickness (nm), (3) Lna: NMOS access transistor channel length (nm), (4) L_{pa}: PMOS access transistor channel length (nm), (5) W_{na}: NMOS access transistor channel width (nm), (6) W_{pa}: PMOS access transistor channel width (nm), (7) L_{nd}: NMOS driver transistor channel length (nm), (8) W_{nd}: NMOS driver transistor channel width (nm), (9) L_{pl}: PMOS load transistor channel length (nm), (10) W_{pl}: PMOS load transistor channel width (nm), (11) N_{chn}: NMOS channel doping concentration (cm^{-3}), (12) N_{chp}: PMOS channel doping concentration (cm^{-3}). Amongst these parameters some are independent and others are correlated which is to be considered during the simulation [14].

TABLE III
THE RESULTS FOR THE PROPOSED APPROACH AT 65NM TECHNOLOGY AND A TYPICAL CORNER

Circuit	# of gates	Function	leakage power (65 nm)						% leakage power reduction (65nm)		
			Non optimized (uw)			Optimized (nw)					
			T=25°c	T=50°c	T=100°c	T=25°c	T=50°c	T=100°c	T=25°c	T=50°c	T=100°c
C432	160	27- channel interrupt controller	3.839	4.13	7.480	81.92	84.79	105.6	98%	98%	98.6%
C499	202	32- bit SEC circuit	4.876	6.651	12.65	84.25	102.7	117.5	98.4%	98.46%	99%
C1355	546	32- bit SEC circuit	7.721	10.53	18.08	154.1	194.4	337.1	98%	98.15%	98.17%
C1908	880	16- bit SEC/DED	13.79	17.21	23.14	177.9	186.4	220.8	99.15 %	98.95%	99%



(a)



(b)

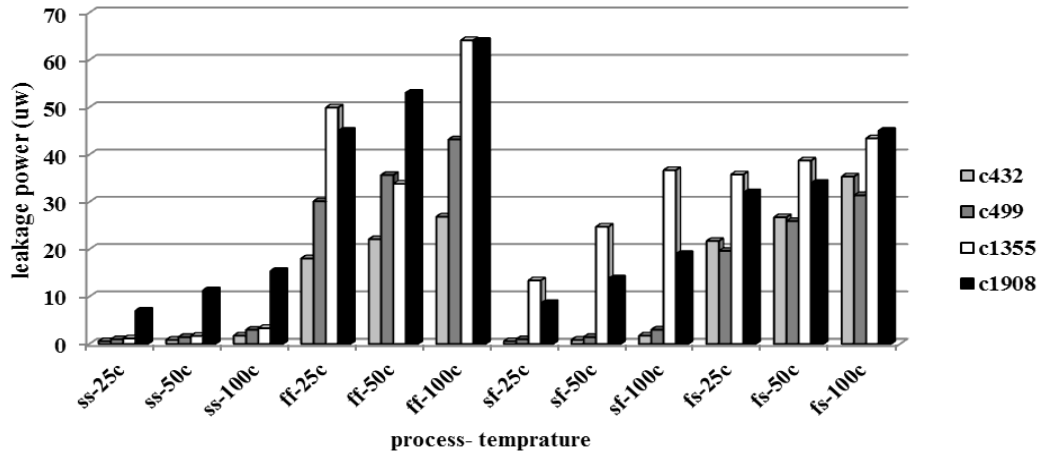
Fig. 5 Standby power dissipation of the ISCAS'85 circuit in different
Process-corner and temperature conditions (s: slow corner, f: fast corner), in 32nm technology
(a) without optimization; (b) with optimal V_{BODY}

To demonstrate the proficiency of the system, it is implemented and simulated in 32nm and 65nm technology at different process-corner conditions (SS, FF, SF and FS) and at different temperatures. Fig. 5 (a) illustrates the leakage power dissipation of each benchmark circuits at different process-corner conditions and different temperatures in 32nm, by

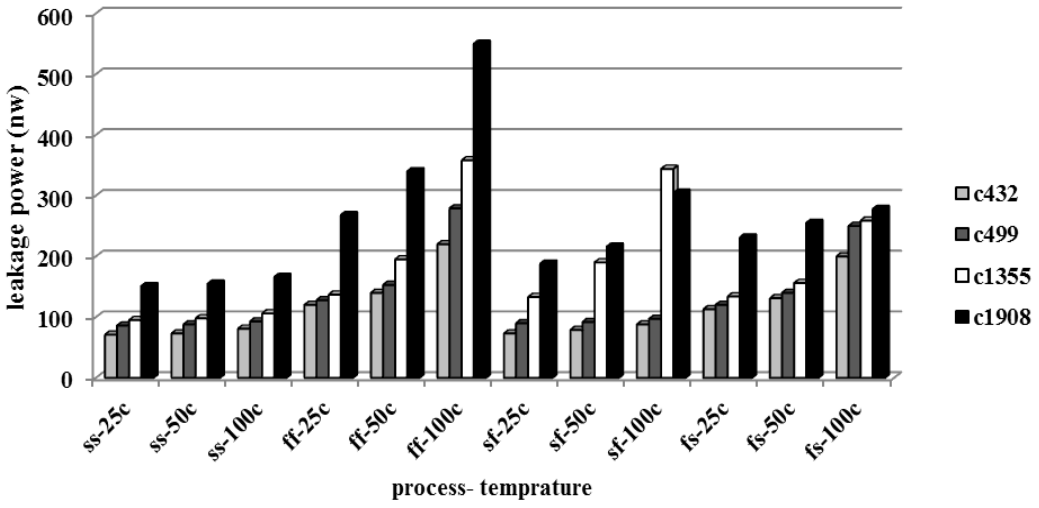
applying our proposed monitor and control body bias circuit to these benchmark circuits, as experimental results expression in Fig. 5 (b), the proposed system is very effective and practicable in reducing the standby power in the big circuits with the minimal hardware overhead of transistors and the minimal power overhead (10-12 uW).

In the case of nanoscale circuit process variation maintaining the circuit yield is the most important design challenge, when the proposed technique is applied to the chip core besides the circuit yield safeguard, the leakage power dissipation is approximately insensitive to the temperature and process corner variations. As mentioned before, since the optimal body bias voltage was changed, this in situ monitoring circuit automatically revolves according to the new temperature and process.

Fig. 6 (a) shows the summary of the results for the benchmark without optimization, and Fig. 6 (b) shows the summary of the results for the proposed approach at different operating temperature ranges, from 25 ◦C to 100 ◦C and variation in process corner in 65nm technology. Analysis of the results shows that at least 98% up to the maximum of 99.55% reduction in leakage power consumption is achieved from the proposed method.



(a)



(b)

Fig. 6 Standby power dissipation of the ISCAS'85 circuit in different Process-corner and temperature conditions (s: slow corner, f: fast corner), in 65nm technology (a) without optimization; (b) with optimal V_{BODY}

Finally a briefly comparison has been defined in Table IV, which consider the overhead power of previous monitor circuits which present in references, notice that resolution and power reduction percentage for each circuit is different. However it is notable, the overhead of proposed circuit reduces at least about 75% to compare with similarity ones. For more information it is better to refer to the related paper.

TABLE IV
COMPARISON OF POWER MONITOR OVERHEAD

circuit	technology	overhead power
Proposed circuit	65 nm	12 μW
Proposed circuit	32 nm	10 μW
[3]-[7]	32nm	41 μW
[8]	32nm	141 μW
[1]-[4]	90 nm	244 μW
[10]	45 nm	30 μW

V. CONCLUSION

The desire for higher transistor densities and faster devices trend the technology scaling goes down. As the threshold voltage is reduced along with device dimensions, a large standby or "off' current is consumed even though no logic operations are being performed. Therefore, the new circuit design technique is necessary to minimizing this critical issue. Reverse substrate bias in the standby mode is one of the best techniques to overcome this problem.

In this paper we have described a monitoring scheme for minimizing power consumption by means of V_{BODY} control in standby mode. Our approach considering the total leakage components, moreover uses the simple blocks which offer good sensitivity, high speed, the continuously feedback loop and the most important ones low-power overhead, which reduces at least about 75% to compare with the other monitoring circuits.

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