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A Current-mode Continuous-time Sigma-delta Modulator based on Translinear Loop Principle

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***Abstract*—**In this paper, a new approach for design of a fully differential second order current mode continuous-time sigma-delta modulator is presented. For circuit implementation, square root domain (SRD) translinear loop based on floating-gate MOS transistors that operate in saturation region is employed. The modulator features, low supply voltage, low power consumption (8mW) and high dynamic range (55dB). Simulation results confirm that this design is suitable for data converters.

***Keywords*—**Sigma-delta, current-mode, translinear loop, geometric mean, squarer/divider.

I. Introduction

THE increased use of CMOS integrated circuit in digital signal processing has led to the request for methods of analog-to-digital and digital-to-analog conversion that can be implemented in standard CMOS technologies. The oversampled techniques of the sigma delta conversion are in interest since they allow high-resolution without an increase in the matching requirements of the converter components [1,2]. The converters have found in such applications as communications systems, signal processing, wireless systems, consumer and professional audio, industrial weight scales and precision measurement devices. The features of sigma-delta converters are that they are not only the lower cost conversion methods, but also provide both flexibility and high dynamic range in converting low bandwidth input signals. The noise-shaping performance of loop filter distributes the quantization error or noise such that it is very low in the band interest. Therefore, noise shaping achieves relatively high signal-to-noise (SNR) with a simple quantizer.

In recent years, continuous-time (CT) sigma-delta modulators have attracted increasingly because they can work in low power consumption and low voltage operation [1-6]. Moreover, because of placing sampler inside loop filter, charge injection effect and nonlinear sampling switched on resistances are significantly suppressed. In addition, the continuous time loop filter attenuating out of band high frequency interferers before sampling act as an anti-alias filter.

In this work, we present a CT sigma delta modulator based on SRD loop filters. Integrators of loop filter are implemented using current-mode using squarer/divider and geometric mean units [7] as basic building blocks, which they work in low voltage/low power. The basic units are designed employing FG-MOS transistors with sources connected to the substrate to construct the electronically translinear loop circuit of SRD Integrator. So, the proposed filter is immune to the body effect and with very low voltage with minimum of one V_{gs} plus one V_{ds} .

The rest of paper is organized as follows. Section II reviews theoretical operation of the proposed sigma-delta modulator. In section III detailed circuits implementation is presented. Simulation results of designed sigma-delta modulator are described in section IV. Finally, conclusion is provided in section V.

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II. Theoretical Operation

Fig. 1 shows a general block diagram of a CT sigma-delta modulator. Using impulse invariant transformation for a second order low-pass loop filter of a sigma-delta modulator H(s), the following transfer function is achieved [8] as:

$$H(s)=\frac{(1+1.5Ts)}{(Ts)^2} \tag{1}$$

where, T is the period of the sampling.

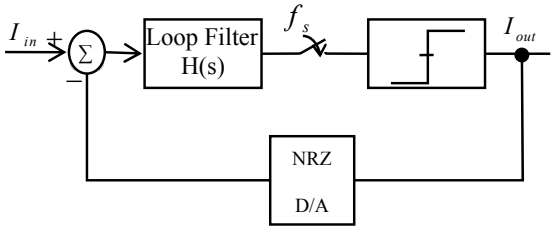


Fig. 1 Block diagram of a CT sigma-delta modulator

To design of the loop filter many proposals such as transconductance and capacitance (gm-C), hybrid active-passive loop filter and switch current is presented[1,5,6 ,8]. In this work SRD loop filter based on translinear loop is employed. Fig. 2 shows single ended block diagram of a loop filter based on (1). To this end, state-space equations of transfer function (1) will be expressed as:

$$\begin{cases} T\dot{I}_1 = I_{in} \\ T\dot{I}_{out} = 1.5I_{in} + I_1 \end{cases} \tag{2}$$

where I_1 is internal state space variable and I_{in} and I_{out} are the input and output signals.

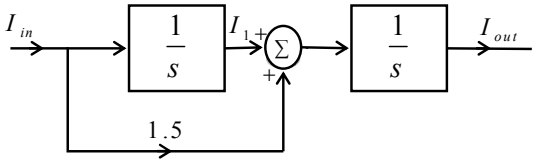


Fig 2. Block diagram of a second order loop filter

III. CIRCUIT DESIGN

A. Loop filter

In order to design current mode SRD loop filter a nonlinear transform will be performed. In this work, the quadratic behavior of MOS transistor, which operates in strong inversion mode, is used. To design, we start with the analysis of the circuit shown in Fig. 3. Assuming that the M1 work in saturation mode, relationship between output current I_{out} and capacitor voltage V_{cap} can be expressed as:

$$I_{out} = \frac{\beta}{2}(V_{cap} - V_{th})^2 \tag{3}$$

where $\beta=\mu_o C_{ox}(W/L)$ is the transconductance parameter of transistor, μ_o is the electron mobility, C_{ox} is the gate oxide capacitance and W/L is the aspect ratio of transistor.
By taking derivation of (3) it is obtained:

$$\dot{I}_{out} = \sqrt{2\beta I_{out}}\,\dot{V}_{cap} \tag{4}$$

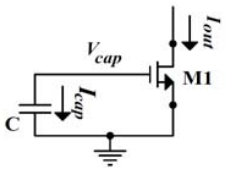


Fig. 3. SRD integrator principle

Substituting (4) in (2) and then multiplying C in both sides of all equations, it results:

$$\begin{cases} C_1\dot{V}_1 = \dfrac{C_1}{\sqrt{2\beta T}}\dfrac{I_{in}}{\sqrt{I_1}} \\ C_2\dot{V}_2 = \dfrac{C_2}{\sqrt{2\beta T}}\left(\dfrac{1.5I_{in}}{\sqrt{I_{out}}} + \dfrac{I_1}{\sqrt{I_{out}}}\right) \end{cases} \tag{5}$$

Fig. 4 shows, block diagram of the single ended implementation of above equations. From this figure it can be seen that essential part of the circuit is geometric-mean function (and also, squarer/divider function which is inverse function of geometric-mean).

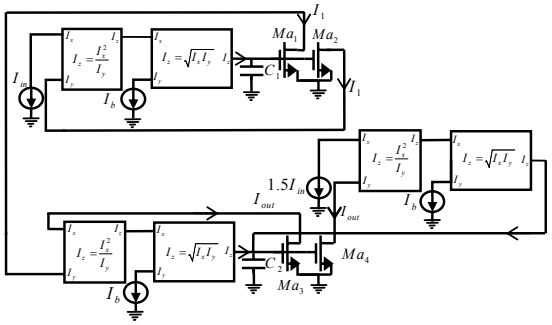


Fig. 4 Block diagram of SRD domain second order loop filter

In this work, for circuit implementation of geometric-mean function, SRD translinear loop based on floating gate MOS (FG-MOS) is employed. Fig. 5 shows symbol diagram of a FG-MOS with two input capacitance connection in gate and its equivalent circuit diagram.

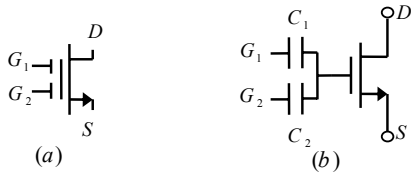


Fig. 5 FG-MOS transistor a) symbol b) equivalent circuit

Neglecting the parasitic capacitance and residual charge trapped, the drain current of the FG-MOS transistor with two input gate in saturation region and $C_1=C_2$, is given by [7]:

$$I_D = \frac{\beta}{2}(\tfrac{1}{2}V_1 + \tfrac{1}{2}V_2 - V_{th})^2 \tag{6}$$

where, V_1 and V_2 are input gate voltages.

A basic current mode SRD translinear loop circuit employing FG-MOS transistor is shown in Fig. 6.

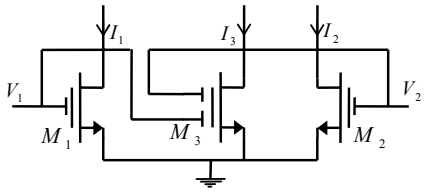


Fig. 6 Basic circuit design of current mode SRD translinear loop

Assuming $\beta_3 = 4\beta_1 = 4\beta_2 = \beta$, the drain current of transistors M1, M2 and M3 are given as following:

$$\begin{cases} I_1 = \frac{\beta}{4}(V_1 - V_{th})^2 \\ I_2 = \frac{\beta}{4}(V_2 - V_{th})^2 \\ I_3 = \beta(\frac{1}{2}V_1 + \frac{1}{2}V_2 - V_{th})^2 \end{cases} \quad (7)$$

Combination of I-V relationships of transistors is obtained as:

$$\sqrt{I_3} = \sqrt{I_1} + \sqrt{I_2} \quad (8)$$

Squaring both side of equation (8) it results:

$$I_3 = I_1 + I_2 + 2\sqrt{I_1 I_2} \quad (9)$$

Therefore, for certain current injections of transistor M_3, equation (9) will be converted to:

$$I_3 = \sqrt{I_1 I_2} \quad (10)$$

Therefore, geometric-mean circuit is obtained by taking I_1 and I_2 as input currents and I_3 as the output current, which is shown in Fig. 7 [7].

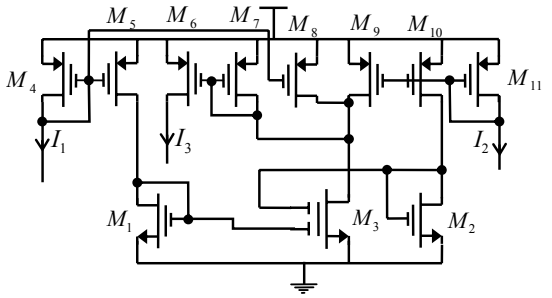


Fig. 7 Current mode geometric mean circuit

From Fig. 7 the sources and the body of the transistors are connected to the ground so the body effect is completely eliminated. The minimum supply voltage needed to properly bias the circuit is one V_{ds} plus one V_{gs}, so this circuit is suitable for low voltage application. In addition, comparing with previously reported circuits, complexity of the circuit is decreased.

The squarer/divider is obtained after few modifications on Fig. 7 by taking I_1 and I_3 as input currents and I_2 as the output current.

As Fig. 4 shows, the capacitors of the filter cannot be discharged without using CMFB circuits [7]. In this proposal differential pair is used, in which each capacitor of each half circuit is discharged by using of the counterpart state variable in the other half circuit [7]:

B. Current mode comparator and DAC

The circuit of a one bit comparator plus one bit DAC, which is a part of the modulator, is shown in Fig. 8. This comparator uses a buffer at the front stage [9]. An inverter provides a positive feedback, that results fast response and low input resistance. The input current comparator I_{in} is actually the difference between input current and feedback current (which is the same reference current). The circuit works in two modes. When input current I_{in} is positive, node V_1 is pulled high and inverter amplifies V_1, and V_2 goes low. V_1 has low impedance because M_1 is on and M_2 is off. When input current I_{in} is negative, node V_1 is pulled low, resulting low voltage for V_2. In later case similarly, V_1 has low impedance because M_1 is off and M_2 is on. At the back stage of circuit a one bit DAC is used, which implemented with two switches and one current source that current directed via switches that are controlled by the output of the comparator.

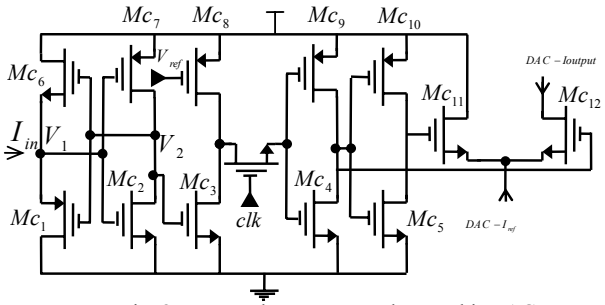
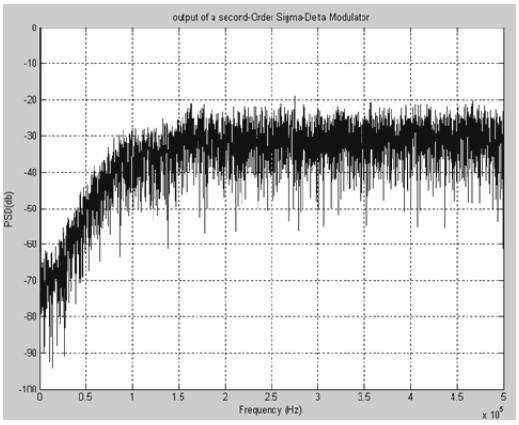


Fig. 8 Proposed comparator plus one bit DAC

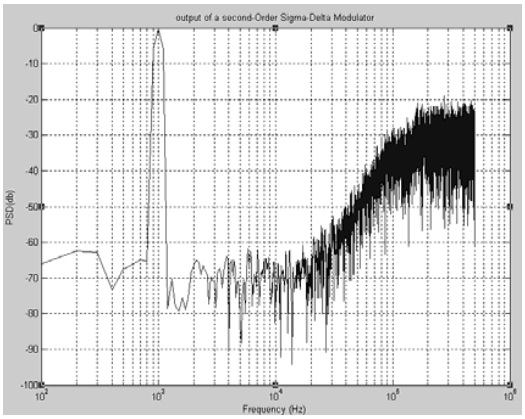
IV. Simulation Results

A second order sigma delta modulator based on the block diagram of Figs. 1, 2 and the proposed translinear loop of Fig. 4 was designed. The circuit was simulated with TSMC 0.18um CMOS technology ≅ (V_{thn}≅+0.45V and V_{thp}≅-0.56V), with V_{dd}=1.8V, capacitors C=1nF, C_1=C_2=0.75nF, I_b=4μA, DAC-I_{ref}=20μA and V_{ref}=0.85V were employed. The aspect ratios of the NMOS and PMOS transistors for the loop filter were 30μm/5μm and 40μm/5μm, respectively. For the FG-MOS transistor, it was 60μm/5μm. For the quantizer and DAC, the aspect ratios of the NMOS and PMOS transistors were 0.3μm/0.18μm and 0.36μm/0.18μm, respectively. A sinusoidal current input with amplitude of 20μA and frequency of 1KHz was applied for input of modulator. The sampling frequency was set 1 MHz the oversampling ratio (OSR), is 64. The output data of the modulator were collected, and then FFT with hanning window was used to evaluate SNR and power spectral density (PSD). Fig. 9 shows the power spectrum of the modulator. Fig. 10 shows Signal-to-Noise vs. input amplitude and the maximum SNR (including distortion) is 55dB, therefore the bit resolution is 9bit for the proposed modulator.

Simulation results showed the power consumption of less than 8mW for maximum accepted currents. The characteristics of the proposed second-order CT sigma-delta modulator are summarized in table I.



(*a*)



(*b*)

Fig. 9 Power spectrum of the proposed sigma-delta
a) out band b) in band

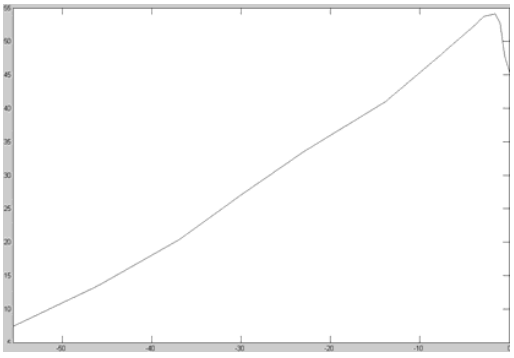


Fig. 10 Signal-to-Noise vs. input amplitude

TABLE I
CIRCUIT CHARACTERISTICS

Technology	0.18u CMOS
Supply Voltage	1.8V
Power Consumption	8mW
Dynamic Range	55dB
Sampling Frequency	1 MHz
Oversampling Ratio	64
Order of loop filter	2nd
Bit Resolution	9bit

V. CONCLUSION

A low voltage fully differential sigma-delta modulator based on SRD translinear loop is presented. The circuit works in current-mode and employs FG-MOS transistors that operate in saturation region. Simulation results of a modulator show that the technique is promising and can be used in low voltage data converters.

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