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A Simulation Model for the H-gate PDSOI MOSFET

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***Abstract*—**The floating body effect is a serious problem for the PDSOI MOSFET, and the H-gate layout is frequently used as the body contact to eliminate this effect. Unfortunately, most of the standard commercial SOI MOSFET model is for the device with finger gate, the necessity of the new models for the H-gate device arises. A simulation model for the H-gate PDSOI MOSFET is proposed based on the 0.35μm PDSOI process developed by the Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS), and then the model is well verified by the ring-oscillator.

***Keywords*—**PDSOI H-gate Device model Body contact.

I. Introduction

SOI technologies have been very attractive for future high-speed operation of CMOSFETs [1]. However, because of the floating body effect, SOI devices exhibit premature bipolar conduction which coupled with the increase in the body voltage causes the kink seen in the output characteristics of partially depleted (PD) SOI n-MOSFETs [2]. There are many techniques to eliminate the kink effect[3], among which the body contact has been regarded as a complete cure for this problem, and the H-gate layout is frequently used. However, most of the standard SOI MOSFET model is for the device with finger gate, while some have considered the device with body contact but the body contact effect is not considered completely, even in the newest BSIMSOI MODEL BSIMSOIV4.4 [4-6].

In this paper, we present a simulation model for the H-gate PDSOI MOSFET based on the 0.35μm PDSOI process developed by the Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS), and then this model is well verified by the ring-oscillator.

II. Model Building

The PDSOI MOSFET with H-gate was fabricated using the 0.35μm SOI process developed by the Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS). They were fabricated on UNIBOND SOI wafers, and the simplified layout is shown in Fig.1. The H-gate NMOS is taken as an example in the Model building, and the modeling of PMOS is the same with NMOS.

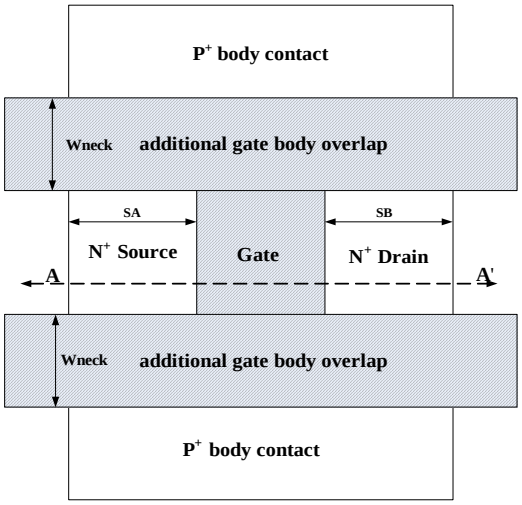

Fig. 1 The simplified layout of H-gate MOSFET

Compared with the finger gate device, the H-gate device has additional gate body overlap region which is shown in Fig.1, which imports the additional gate-to-body capacitance that was called Cadd in this paper. The width of this capacitance is Wneck, which is the width of the neck of the H-gate as shown in Fig.1, and the length of the capacitance is equal to 'SA+L+SB'. This capacitance is changeless for the devices with the same length, and it will greatly degrade the performance of the device when the width of the device is narrow.

The additional gate body overlap region also imports PN junctions between the source and the bulk that under this region at the vertical of the source, and also between the drain and the bulk. These PN junctions should be defined by the perimeter because they are lateral junctions, and the perimeter of the PN junctions is equal to the parameters *SA* and *SB* separately.

Unlike the commercial process, the diffusion of the source and drain don't touch the buried oxide (BOX) in our process, which is shown in Fig. 2. So there lies PN junction between the source and bulk at the bottom of the source, and also at the bottom of the drain. However, these PN junctions are not considered in the standard SOI MOSFET model. The area of these PN junctions is equal to the area of the source and drain separately, which can be extracted from the Layout Post Extract (LPE).

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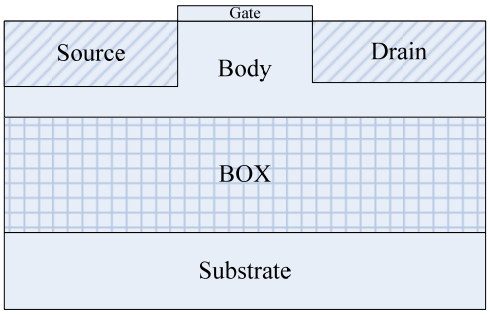

Fig. 2 The cross-sectional view of Fig.1 along AA'

Based on the analysis above, the equivalent circuit of the H-gate SOI MOSFET is shown in Fig. 3. The bottom junction and vertical junction are integrated into a PN junction in this circuit, and they are determined by the parameters *area* and *pj* separately.

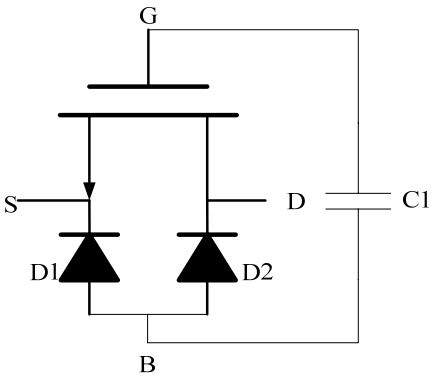

Fig. 3 The equivalent circuit of the H-gate SOI MOSFET

This model can easily be implemented in the standard SOI MOSFET model BSIMSOI as a macro-model for the circuit simulation, and the code is as follows:

*.subckt Hgate_nmos d g s e b w=3.5u l=0.35u as='w*8e-7' ps=2*'w+8e-7' ad='w*8e-7' pd=' 2*'w+8e-7' SA=8e-7 SB=8e-7 Wneck=0.35u*

M1 d g s e b nmos w=w l=l as=as ps=ps ad=ad pd=pd
*D1 b s pwell area=as pj='2*SA'*
*D2 b d pwell area=ad pj='2*SB'*
*Cadd g b '2*Wneck*(SA+L+SB)*C_{unit} '*
.end Hgate_nmos

where the parameters *as, ps, ad, pd, Wneck, SA* and *SB* are all layout dependent parameters，they can all be extracted from LPE. C_{unit} is the unit capacitance of the capacitance between gate and body. The model *nmos* is the standard SOI MOSFET model, and *pwell* is the standard diode model. The parameters of *nmos* and the parameters of *pwell* should be extracted before the use of this model.

III. Model Verification

We've extracted the parameters of the SOI MOSFET model *nmos* and the diode model *pwell* with the Model Builder Program (MBP), and we also extracted the parameters of the PMOS for the circuit simulation. A 101-stage ring-oscillator is used as the validate circuit. The schematic circuit is shown in Fig.4, the width of the PMOS for the inverter is 10um, and the width of the NMOS is 5um. We've measured and simulated the period of the ring-oscillator, and the results are shown in Table I, these results validate the accurate of the model well.

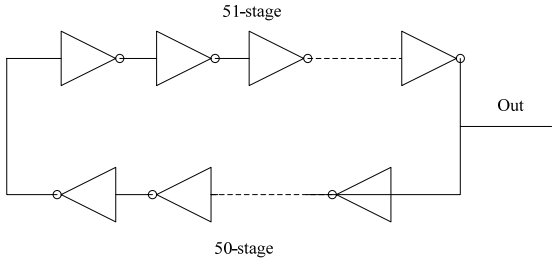

Fig. 4 The schematic circuit of the 101-stage ring-oscillator

TABLE I
The Measured and Simulated Period

validate circuit	Test period	Simulated period With standard model	Simulated period With H-gate model
101-stage ring-oscillator	12ns	9.5ns	12.4ns

IV. Conclusion

A simulation model for the H-gate SOI MOSFET is proposed based on the 0.35μm SOI process developed by IMECAS. The bottom PN junction, vertical PN junction and the additional gate-to-body capacitance that are caused by the body contact are added in this model, and then this model is well verified by the ring-oscillator.

References

[1] C. Chun-Yen, et al. Reduced reverses narrow channel effect in thin SOI nMOSFETs. Electron Device Letters, IEEE, 2000,vol. 21, pp. 460-462
[2] A. Daghighi and M. A. Osman. Two-dimensional model for investigating body contact structures in PD SOI MOSFETs. Microelectronic Engineering, 2003, vol. 70, pp. 83-92

[3] C. Xiaowu and H. Chaohe. Study of body contact of partial depleted SOI NMOS devices. 8th International Conference on Solid-State and Integrated Circuit Technology, 2006, pp. 212-214.
[4] BSIMSOIv4.4 MOSFET MODEL Users' Manual, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720.
[5] P. Su, S. K H. Fug, et al. A Body-Contact SO1 MOSFET Model for Circuit Simulation. 1999 IEEE International SO1 Conference, 1999, pp.50-51
[6] M. Mochizuki, et al. Accurate and global model of SOI H gate body-tied MOSFET for circuit simulator.2011 International conference on Simulation of Process and Device.2011,pp.247-250

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