

# Characterization of the LMOS with Different Channel Structure

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**Abstract**—In this paper, we propose a novel metal oxide semiconductor field effect transistor with L-shaped channel structure (LMOS), and several type of L-shaped structures are also designed, studied and compared with the conventional MOSFET device for the same average gate length ( $L_{avg}$ ). The proposed device electrical characteristics are analyzed and evaluated by three dimension (3-D) ISE-TCAD simulator. It can be confirmed that the LMOS devices have higher on-state drain current and both lower drain-induced barrier lowering (DIBL) and subthreshold swing (S.S.) than its conventional counterpart has. In addition, the transconductance and voltage gain properties of the LMOS are also improved.

**Keywords**—Average gate length ( $L_{avg}$ ), drain-induced barrier lowering (DIBL), L-shaped channel MOSFET (LMOS), subthreshold swing (S.S.).

## I. INTRODUCTION

RECENTLY, bulk Silicon device has faced a scaling down challenge [1]-[4]. In order to overcome this issue, the research of vertical MOSFET and FinFET has been concerned. But these structures are all straight-line channel device, which always focuses on severe short-channel effects (SCEs) such as large drain induce barrier lowering (DIBL) and large leakage current. Also, the self-alignment requirement is strongly concerned for the short channel device. Therefore, the non-straight-line channel device has been studied [5]. However, there is no paper analyzing the electrical factors for non-straight-line channel devices with different channel structure. In this work, we propose five different channel structures of L-shaped MOSFETs named LMOS, which have the same average channel length ( $L_{avg}$ ) but smaller drain side channel length ( $L_d$ ) as shown in Fig. 2. It is worthwhile noting that the fabrication of LMOS devices and conventional MOSFETs are the same. That means L-shaped MOSFETs are easy to be made by fully compatible CMOS technology. Compared with a conventional MOSFET with its channel direction of (100) named Con100, the simulation results show that at the different location of the source/drain terminal, LMOS devices possibly increase their on-state drain current ( $I_{on}$ ) and reduce both their drain induce barrier lowering (DIBL) and subthreshold swing (S.S.). On the other hand, the simulation results exhibits that LMOS devices have higher transconductance and voltage gain ( $A_v$ ) compare with a

conventional MOSFET with the same channel direction of (010) named Con010. Furthermore, due to the L-shaped structure reduces the encroachment of the drain electrical-field, LMOS reveals a better gate controllability than the conventional devices do.

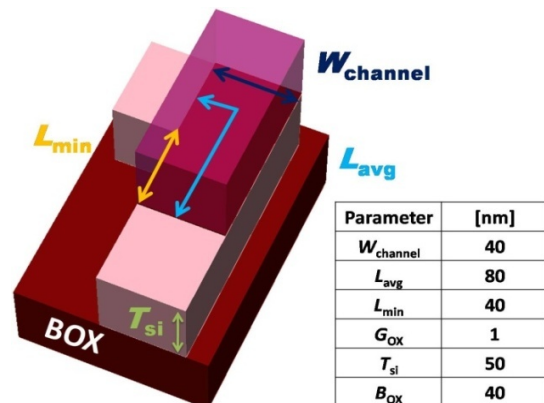


Fig. 1 Schematic of L-shaped channel MOSFET (LMOS). The parameters for LMOS are  $W_{channel}=40\text{nm}$ ,  $L_{avg}=80\text{nm}$ ,  $L_{min}=40\text{nm}$ ,  $G_{ox}=1\text{nm}$ ,  $T_{si}=50\text{nm}$ , and  $B_{ox}=40\text{nm}$

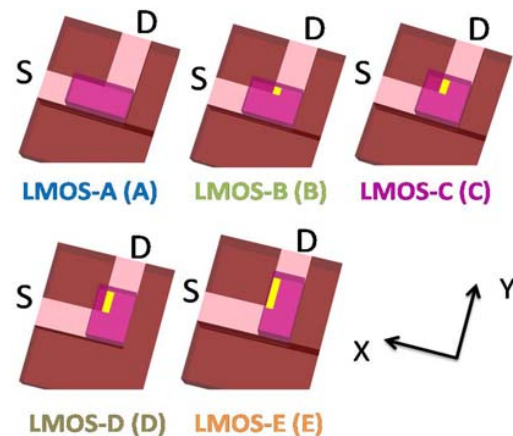


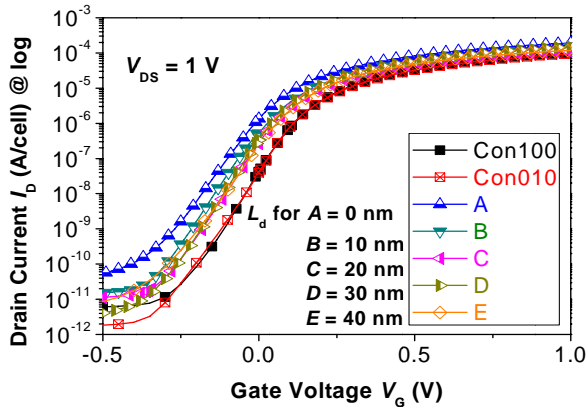
Fig. 2 Different types of LMOS with channel parallel X-Y axis and  $L_d=(A) 0\text{nm}$ , (B)  $10\text{nm}$ , (C)  $20\text{nm}$ , (D)  $30\text{nm}$ , (E)  $40\text{nm}$  respectively. The parameters for LMOS are  $W_{channel}=40\text{nm}$ ,  $L_{avg}=80\text{nm}$ ,  $L_{min}=40\text{nm}$ ,  $G_{ox}=1\text{nm}$ ,  $T_{si}=50\text{nm}$ , and  $B_{ox}=40\text{nm}$

## II. SIMULATION DETAILS AND DEVICE STRUCTURE

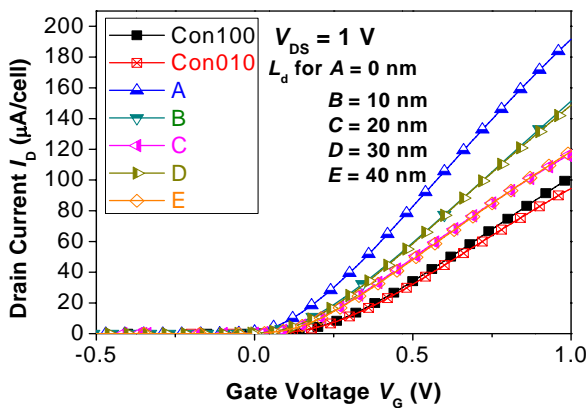
We used ISE-TCAD DEVICE and DESSIS to simulate the devices proposed in this paper as shown in Figs. 1 and 2. The

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generation and recombination models we used including Shockley-Read-Hall (SRH), auger avalanche, and band-to-band tunneling (BTBT). The substrate that we used was  $T_{si} = 50\text{nm}$  Silicon film thickness on the top of a  $40\text{nm}$  BOX with channel width  $W_{channel} = 40\text{nm}$ . The minimum gate length ( $L_{min}$ ) of LMOS devices are  $40\text{nm}$  and their average gate length ( $L_{avg}$ ) are all  $=80\text{nm}$ , which is doped  $2 \times 10^{18}\text{cm}^{-3}$  (boron). N-type doping in source/drain is the same at  $1 \times 10^{20}\text{cm}^{-3}$  (Arsenic). It should be noted that all LMOS and conventional devices in this paper have same  $L_{avg}$  but different  $L_d$  which is the length from drain terminal to the corner of L-shape and we named it as the drain side channel length ( $L_d$ ).



(a)



(b)

Fig. 3 Simulated  $I_D$ - $V_G$  curves for the conventional and LMOS devices with  $V_{DS}=1\text{V}$

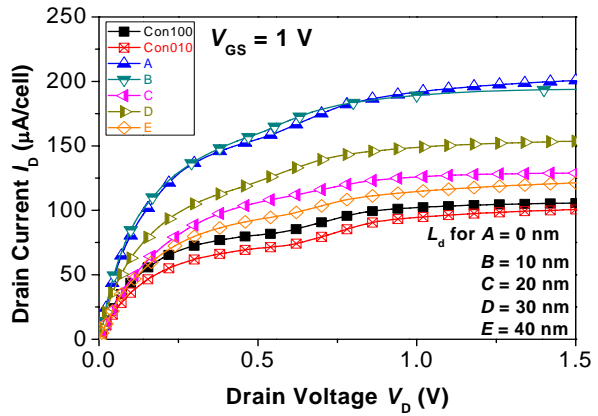


Fig. 4 Simulated  $I_D$ - $V_D$  curves for the conventional and LMOS devices with  $V_{GS}=1\text{V}$

### III. RESULTS AND DISCUSSION

Fig. 3 shows the  $I_D$ - $V_G$  characteristics of traditional devices and LMOS devices with  $V_{DS}=1\text{V}$ . It is clear that LMOS have higher on-state drain current ( $I_{on}$ ) compared with the traditional devices. Because L-shaped MOSFETs have smaller drain side channel length ( $L_d$ ) at the same average channel length ( $L_{avg}$ ) and at the same body volume, the electron is easy to pass the channel and it cause higher  $I_{on}$ .

Fig. 4 shows the  $I_D$ - $V_D$  characteristics of LMOS devices at  $L_{avg} = 80\text{nm}$ . It is observed that the drain current ( $I_D$ ) of L-shaped MOSFETs are higher than that of conventional devices with  $V_{GS}=1\text{V}$ . As we know the current ( $I$ ) is defined as  $I = V / R$ . Thus, when the drain side channel length ( $L_d$ ) is getting longer the resistance of the  $L_d$  ( $r_{dc}$ ) is decreased. Also, the drain current of LMOS is higher than those of the conventional devices.

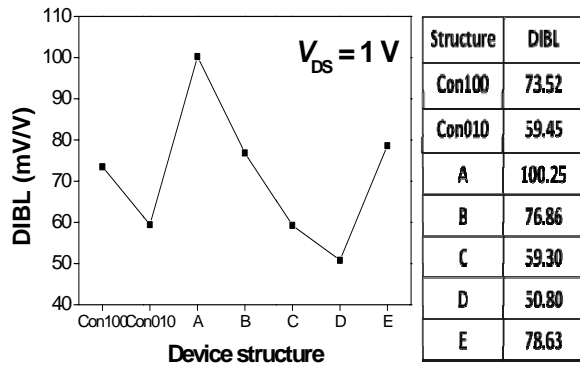


Fig. 5 The DIBL characteristics of conventional and LMOS devices with  $V_{DS}=1\text{V}$

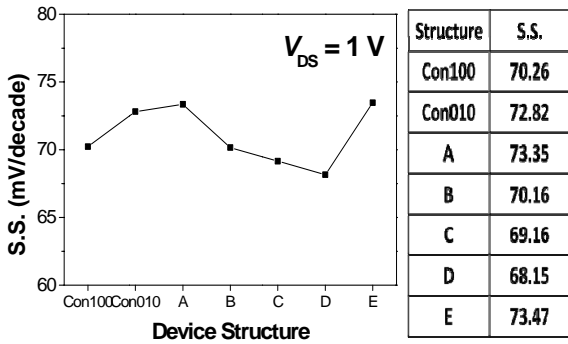


Fig. 6 The S.S. characteristics of conventional and LMOS devices with  $V_{DS}=1$  (V)

Fig. 5 shows the simulation results of DIBL effect. Here, it is easy to perceive the contrast between straight-line channel and L-shaped channel. Although Con010 and LMOS-E (E) has equivalent  $L_{avg}=80\text{nm}$  and parallel channel, E has the shortest channel length between drain and source, which is  $L_d=40\text{nm}$ . Because of the short channel effects (SCEs), the DIBL of the LMOS-E is higher than Con010. On the other hand, LMOS-A has a shorter source side channel length named  $L_s=40\text{nm}$  and Con100 has only average channel length  $L_{avg}=80\text{nm}$ . Due to the SCEs, the DIBL of the LMOS-A is high. Compared to A, E, LMOS-B (B), LMOS-C (C), and LMOS-D (D) when channel structure is winding, drain voltage is not easy to impact source so that the DIBL induced in turn for the B, C, and D, structures are lower than those of A and E structures.

The subthreshold swing (S.S.) is plotted in the Fig. 6. When the MOSFET devices depletion area is increased,  $V_G$  is difficult to control the carrier in the channel and the S.S. is increased. In these LMOS devices, when the drain side channel length ( $L_d$ ) is getting longer, the depletion area at the drain side is decreased. For this reason, as the  $L_d$  is extended, the S.S. is also decreased.

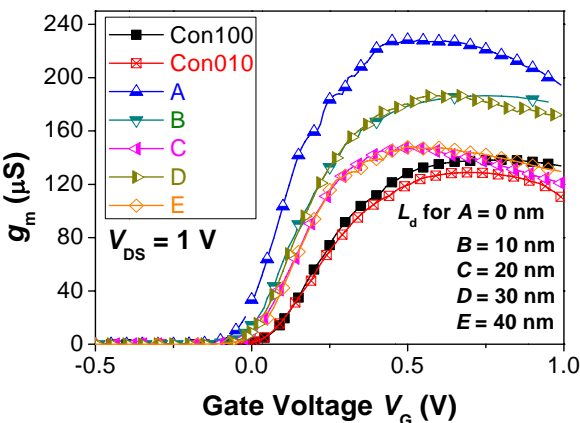


Fig. 7 The  $g_m$ - $V_G$  characteristics of conventional and LMOS devices with  $V_{DS}=1$  (V)

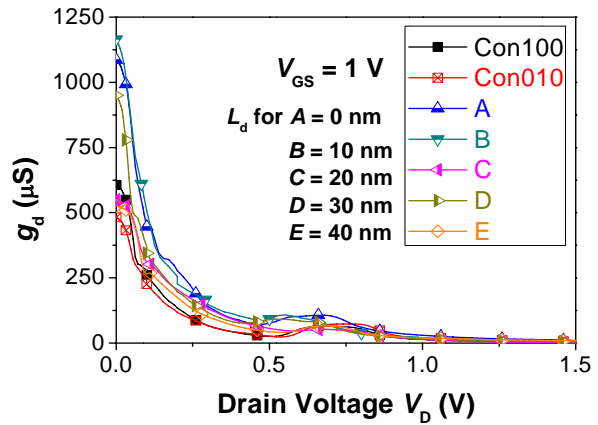


Fig. 8 The  $g_d$ - $V_D$  characteristics of conventional and LMOS devices with  $V_{GS}=1$  (V)

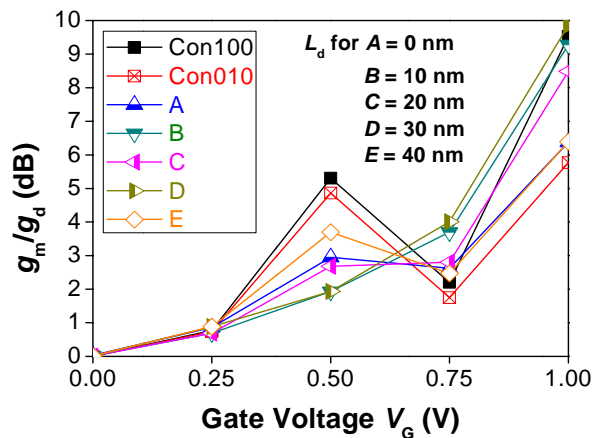


Fig. 9 The  $g_m/g_d$  versus  $V_G$  characteristics of conventional and LMOS devices with  $V_{DS}=1$  (V)

Fig. 7 presents the  $g_m$ - $V_G$  characteristics of the conventional and LMOS devices. Because LMOSs have  $L_d$  regions, the gate controllability over the depletion region is better than those of conventional devices. Therefore, the  $g_m$  characteristics of LMOSs are improved.

Fig. 8 shows the  $g_d$ - $V_D$  characteristics of the conventional and LMOS devices. When  $V_D$  is small, the value of  $g_d$  is become higher for each devices. Because the  $I_D$  of LMOS devices are larger than those of the traditional device, a bigger value of  $g_d$  is observed. On the other hand, we know that the  $r_o$  is defined as  $r_o = 1 / g_d$ . For this reason, as the  $g_d$  of the LMOS becomes larger, the value of the  $r_o$  is smaller than the conventional one.

Fig. 9 demonstrates the  $g_m/g_d$  versus  $V_G$  characteristics of the conventional and LMOS devices with  $L_{avg}=80\text{nm}$ . This is the most important analog parameter of the devices. It is observed that the highest value of voltage gain ( $A_v$ ) is the LMOS-D, and other device's  $A_v$  are higher than Con010. It means that the L-shaped channel structures are of a good method to reduce DIBL effect and increase device current drive  $I_D$ .

#### IV. CONCLUSION

In this work, we have analyzed the characteristics of five different devices with L-shape channel called LMOS. According to the 3D simulation result, such as  $I_{ON}$ , DIBL, and S.S. of LMOS are better than those of the conventional counterpart. This can be attributed to the location and orientation of the multi-type source/drain terminals. In addition, owing to the  $g_m$  and  $A_{vi}$  of LMOS are significantly increased, these L-shape channel schemes can be used for the nano CMOS technology to increase device performance and system integration density with reduced short-channel effect.

#### ACKNOWLEDGMENT

The authors would like to thank the National Center for High-performance Computing (NCHC) for computer time and facilities.

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