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Optimization of HALO Structure Effects in 45nm p-type MOSFETs Device Using Taguchi Method

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***Abstract*—** In this study, the Taguchi method was used to optimize the effect of HALO structure or halo implant variations on threshold voltage (V_{TH}) and leakage current (I_{Leak}) in 45nm p-type Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) device. Besides halo implant dose, the other process parameters which used were Source/Drain (S/D) implant dose, oxide growth temperature and silicide anneal temperature. This work was done using TCAD simulator, consisting of a process simulator, ATHENA and device simulator, ATLAS. These two simulators were combined with Taguchi method to aid in design and optimize the process parameters. In this research, the most effective process parameters with respect to V_{TH} and I_{Leak} are halo implant dose (40%) and S/D implant dose (52%) respectively. Whereas the second ranking factor affecting V_{TH} and I_{Leak} are oxide growth temperature (32%) and halo implant dose (34%) respectively. The results show that after optimizations approaches is -0.157V at I_{Leak}=0.195mA/μm.

***Keywords*—**Optimization; p-type MOSFETs device; HALO Structure; Taguchi Method.

I. Introduction

THE Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) has been a popular device as it usually used in digital circuits, microprocessor, memory circuit, and other logic application of many kinds. In order to improve electrical device performance in circuit, MOSFETs have been scaled down successfully over the past few decades [1]. The MOSFET includes a channel of n-type or p-type semiconductor material is accordingly called an NMOSFET or a PMOSFET and for this research, it will only focus in PMOSFET (also commonly PMOS). More than 30 years, the MOSFET have continually been scale down in size in channel length from micrometers to submicrometers and then to submicrometers range following Moore's Law. The channel length of MOSFET is reduced from 100nm to 45nm. The size reduction of the device makes great improvement to MOSFET operation. Present day Metal-Oxide Semiconductor (MOS) process invariability use ion implantation into the channel region, which alters the doping profile near the surface of silicon substrate. Diffusion was used in integrated circuit (IC) fabrication before 1970. Currently doping is mainly done by ion implantation. Ion implantation is processes by which dopant ions are forcefully add into the semiconductor in the form of energetic ion beam injection [2]. The ion implantation process provides much more precise control of doping than the diffusion process [3],[4]. By changing dose, energy and rotation of these implants can change the profile and the electrical characteristics of the MOSFET device [4]. One of the most important physical parameter for MOSFET is its threshold voltage (V_{TH}). V_{TH} is the minimum gate voltage needed to create a channel between source and drain. It can be defined as the minimum voltage for strong inversion to occur [5]. The problem with shrunken transistors to the point where the channel lengths are so short, that a significant amount of current leaks through the source-drain channel, even when the transistor switch is in the off position.

As temperature is increased, the sub-threshold leakage increases exponentially because of a drop in the threshold voltage [6]. To reduce these unwanted current, several things can be done. Leakage current can be reduced by increasing the threshold voltage. Each technique to reduced unwanted current can cause other short channel effect, so the designer must scale appropriately to obtain an optimized device. In this work, an optimization of the process parameter conditions for this device is performed by using Taguchi Method. Taguchi Method is well suited to solve such multiple control factor optimization problems [7]. This method uses a special design of orthogonal arrays to study the entire process parameter space with only a small number of experiments. In the current study, for the design of the experiment with a mixed matrix of 4 process parameters with 3 levels and 2 noise factors with 2 levels, there will be as many as 324 (3^4x2^2) runs of testing if using the conventional full factorial design. The testing of only 36 runs with the Taguchi method greatly reduces the

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number of tests and increases the efficiency.

Using an orthogonal array to design the experiment could help the designers to study the influence of multiple controllable factors on the average of quality characteristics and the variations in a fast and economic way, while using a signal-to-noise (S/N) ratio to analyze the experimental data could help the designers of the product or the manufacturer to easily find out the optimal parametric combinations [8]. Usually, there are three categories of the performance characteristics in the analysis of the S/N ratio, that is, the lower-the-better, the higher-the-better, and the nominal-the-better [9]. The S/N ratio for each level of process parameters is computed based on the S/N analysis. Regardless of the category of the performance characteristic, the larger S/N ratio corresponds to the better performance characteristic [10]. Therefore, the optimal level of the process parameters is the level with the highest S/N ratio. Furthermore, a statistical analysis of variance (ANOVA) is performed to see which process parameters are statistically significant. With the S/N and ANOVA analyses, the optimal combination of the process parameters can be predicted [11],[12].

Finally, a confirmation experiment is conducted to verify the optimal process parameters obtained from the parameter design. This method was combined with SILVACO TCAD tool to aid in design and optimizes the process parameters. SILVACO TCAD tools have 2 parts which is Athena and Atlas. TCAD can lower technology development costs up to 40% by reducing the number of experimental lots and shortening development time considering the rising costs of product development and new wafer fabrication facilities. Athena is used for process simulation in design the device. Meanwhile for ATLAS's tool, it used for device simulation and characterization. It is implemented using modern software engineering practices that promote reliability, maintainability, and extensibility. Products that use the ATLAS Framework meet the device simulation needs of all semiconductor application areas [12],[13].

II. Process and Device Sstructure

Sample used in these experiments were <100> oriented and p-type (boron doped) silicon wafers. N-wells are created starting with developing a 200Å oxide screen on the wafers followed by phosphorus doping. The oxide layer was etched after the doping process was completed. It was followed by annealing process to strengthen the structure. Next, Shallow Trench Isolation (STI) was etched to isolate neighboring transistor. A 130Å stress buffer was grown on the wafer with 25-minute diffusion processes. Then, a 1500 Å nitride layer was deposited using the Low Pressure Chemical Vapor Deposition (LPCVD) process. This thin nitride layer was acted as the mask when silicon was etched to expose the STI area. Photo resistor layer was then deposited on the wafers and unnecessary part will be etched using the Reactive Ion Etching (RIE) process. An oxide layer was grown on the trench sides to eliminate any impurity from entering the silicon substrate. Chemical Mechanical polishing (CMP) was then applied to eliminate extra oxide on the wafers. Lastly, STI was annealed for 15 minutes at 900^{o}C temperature. A sacrificial oxide layer was then grown and etched to eliminate defects on the surface [14].

The gate oxide was grown and a Boron Difluoride (BF_2) threshold-adjustment implanted was done in the channel region through this oxide. The polysilicon gate was then deposited and defined followed by the halo implantation. In order to get an optimum performance for PMOS device, arsenic was doped at a $3.36x10^{13}$ atom cm^{-3}. Sidewall spacers were developed after that process. Sidewall spacers were then used as a mask for source/drain (S/D) implantation. Boron atoms were implanted at a desired concentration to ensure the smooth current flow in PMOS device. Silicide layer was then annealed on the top of polysilicon. The next step in this process was the deposited of Boron Phosphor Silicate Glass (BPSG) layer. This layer will be acted as Premetal Dielectric (PMD), which is the first layer deposited on the wafer surface when a transistor was produced. This transistor was then connected with aluminum metal. After this process, the second aluminum layer was deposited on the top of the Intel Metal Dielectric (IMD) and unwanted aluminum was etched to open the contacts. The procedure was completed after the metallization and etching were performed for the electrode formation and the bonding pads were opened. Once the devices were built with ATHENA, the complete devices can be simulated in ATLAS to provide specific characteristics such as the I_D versus V_{GS} curve. The threshold voltage (V_{TH}) can be extracted from that curve [13],[14].

A. Taguchi Orthogonal L_9 Array Method

Aim of the present study was to determine optimum level of four process parameters i.e. Halo implant dose, Source/Drain (S/D) implant dose, Oxide growth temperature and Silicide Anneal Temperature. Whereas, the two noise factors are sacrificial oxide temperature and annealing process temperature. The values of the process parameter and noise factor at the different levels are listed in Table I and Table II respectively.

TABLE I
PROCESS PARAMETERS AND THEIR LEVELS

Symbol	Process Parameter	Unit	Level 1	Level 2	Level 3
A	Halo Implant Dose	atom cm^{-3}	3.36E13	3.38E13	3.39E13
B	S/D Implant Dose	atom cm^{-3}	6.55E13	6.60E13	6.65E13
C	Oxide Growth Temperature	^{o}C	815	820	825
D	Silicide Anneal Temperature	^{o}C	900	910	950

TABLE II
NOISE FACTORS AND THEIR LEVELS

Symbol	Noise Factor	Unit	Level 1	Level 2
N	Sacrificial Oxide Temperature	°C	950 (N_1)	951 (N_2)
M	Annealing Process Temperature	°C	910 (M_1)	915 (M_2)

In this section, the use of an orthogonal array to reduce the number of experiments for determining the optimal process parameters is reported. Results of the process parameters are studied by using the S/N and ANOVA analyses. Based on the results of the S/N and ANOVA analyses, optimal process parameters for device are obtained and verified. In this research, $L_9(3^4)$ orthogonal array which has 9 experiments was used. The experimental layout for the process parameters using the L_9 (3^4) orthogonal array is shown in Table III.

TABLE III
EXPERIMENTAL LAYOUT ING L_9 (3^4) ORTHOGONAL ARRAY

Exp. No.	Process Parameter level			
	A Halo Implant Dose	B S/D Implant Dose	C Oxide Growth Temperature	D Silicide Anneal Temperature
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

III. RESULT AND DISCUSSION

The electrical characteristics result of the first set experiment that has been done by using ATLAS module was discussed. Beside that, this section also shows the optimization result of PMOS device by using Taguchi Method Approach.

A. Analysis of 45nm PMOS Device

Fig. 1 shows the graph of drain current (I_D) versus gate voltage (V_G) at drain voltage, V_D=-0.05V and V_D=-1.1V for PMOS device [12]. The threshold voltage value is -0.157V. These values are still in range $3.0 \pm 12.7\%$ from the nominal values (-0.15V) [15].

The results of V_{TH} and I_{Leak} were analyzed and processed with Taguchi Method to get the optimal design. The optimized results from Taguchi Method were simulated in order to verify the predicted optimal design.

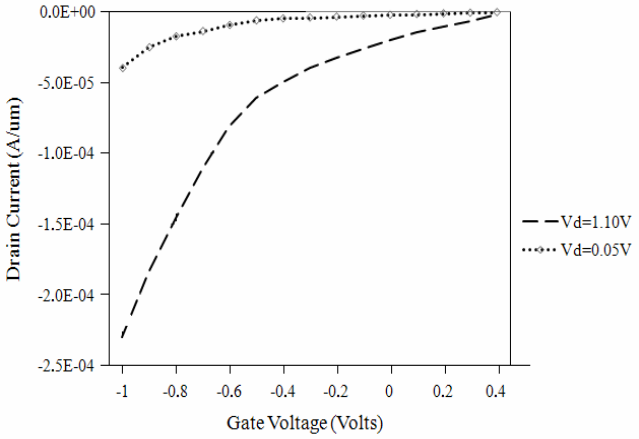

Fig. 1 Graph I_D-V_G for 45nm PMOS Device

B. Analysis of HALO Structure Effects on Threshold Voltage and Leakage Current

The experimental results for V_{TH} and I_{Leak} in PMOS device using the L_9 orthogonal array with two noise factors are shown in Table IV and Table V respectively. In this work, the noise factors were varied for 2 levels as shown in Table II. That is why, we have to get four readings of V_{TH} and I_{Leak} for every row of experiment [7].

TABLE IV
V_{TH} VALUES FOR PMOS DEVICE

Exp. No	Threshold Voltage (Vth)			
	V_{TH} 1	V_{TH} 2	V_{TH} 3	V_{TH} 4
1	-0.1518	-0.1582	-0.1565	-0.1596
2	-0.1466	-0.1491	-0.1496	-0.1425
3	-0.1545	-0.1379	-0.1575	-0.1623
4	-0.1298	-0.1267	-0.1317	-0.1053
5	-0.1358	-0.1186	-0.1378	-0.1387
6	-0.1507	-0.1570	-0.1524	-0.1297
7	-0.1219	-0.1024	-0.1236	-0.1292
8	-0.1352	-0.1415	-0.1370	-0.1361
9	-0.1447	-0.1473	-0.1476	-0.1420

TABLE V
I_{LEAK} VALUES FOR PMOS DEVICE

Exp. No	Leakage Current (μA/μm)			
	I_{LEAK}1	I_{LEAK}2	I_{LEAK}3	I_{LEAK}4
1	0.192	0.196	0.196	0.195
2	0.196	0.195	0.197	0.194
3	0.199	0.190	0.200	0.203
4	0.187	0.186	0.187	0.175
5	0.190	0.181	0.191	0.191
6	0.198	0.199	0.199	0.186
7	0.183	0.174	0.183	0.185
8	0.190	0.192	0.191	0.191
9	0.196	0.195	0.197	0.194

After nine experiments of L_9 array have been done, the next step is to determine, which control factors can gave more effect to a device characteristics. Signal-to-noise (S/N) ratio was used to easily find out the optimal process parameters and analyze the experimental data. There are three categories of performance characteristics in the analysis of the S/N ratio, i.e., the lower-the-best, the higher-the-best, and the nominal-

the-best. In this research, threshold voltage of the 45nm PMOS devices belongs to the nominal-the-best quality characteristics. This S/N Ratio is selected to get threshold voltage value closer or equal to a given target value (0.15V), which is also known as nominal value [16]. The S/N Ratio, η can be expressed as [7]:

$$\eta = 10\mathrm{Log}_{10}\left[\frac{\mu^2}{\sigma^2}\right] \quad (1)$$

Where:

$$\mu = \frac{Y_i + ... + Y_n}{n} \quad (2)$$

$$\sigma^2 = \frac{\sum_{i=1}^{n}(Y_i - \mu)^2}{n-1} \quad (3)$$

While n is number of tests and Y_i the experimental value of the threshold voltage, μ is mean and σ is variance. Leakage current of the 45nm devices belongs to the smaller-the-best quality characteristics. This S/N Ratio is selected to get leakage current value in minimum condition. The S/N Ratio, η of the smaller-the-best quality characteristics can be expressed as [7]:

$$\eta = -10\mathrm{Log}_{10}\left[\frac{1}{n}\sum\left(Y_1^2 + Y_2^2 + ... + Y_n^2\right)\right] \quad (4)$$

Where n is the number of tests and Y_i the experimental value of the leakage current. By applying (1) and (4), the η (S/N Ratio) for each experiment in PMOS device was calculated and given in Table VI.

TABLE VI
S/N RATIOS FOR PMOS DEVICE

Exp. No.	S/N Ratio (dB)	
	Threshold Voltage	Leakage Current
1	33.3	74.21
2	33.1	74.18
3	23.2	74.06
4	20.1	74.71
5	22.9	74.50
6	21.7	74.17
7	20.2	74.83
8	33.8	74.38
9	34.9	74.18

The effect of each process parameter on the S/N Ratio at different levels can be separated out because the experimental design is orthogonal. The S/N ratio (SNR) for each level of the process parameters is summarized in Table VII and Table VIII. In addition, the overall mean SNR for the nine experiments is also calculated and listed in Table VII and Table VIII.

TABLE VII
S/N RESPONSE FOR VTH IN PMOS DEVICE

Symbol	Process Parameter	S/N Ratio (dB)			Overall Mean SNR	Max - Min
		Level 1	Level 2	Level 3		
A	Halo Implant Dose	29.86	21.56	29.64	27.02	8.3
B	S/D Implant Dose	24.51	29.95	26.60		5.44
C	Oxide Growth Temp	29.60	29.37	22.10		7.50
D	Silicide Anneal Temp	30.36	25.00	25.70		5.36

TABLE VIII
S/N RESPONSE FOR ILEAK IN PMOS DEVICE

Symbol	Process Parameter	S/N Ratio (dB)			Overall Mean SNR	Max - Min
		Level 1	Level 2	Level 3		
A	Halo Implant Dose	74.15	74.46	74.46	74.36	0.31
B	S/D Implant Dose	74.58	74.35	74.14		0.44
C	Oxide Growth Temp	74.25	74.36	74.47		0.22
D	Silicide Anneal Temp	74.30	74.39	74.39		0.09

Fig. 2 and Fig. 3 show the S/N ratio graphs of V_{TH} and I_{Leak} for PMOS device respectively. Basically, the larger the S/N ratio, the quality characteristic for the threshold voltage and leakage current are better [7],[8]. The closer the quality characteristic value to the target, the better the product quality will be [16].

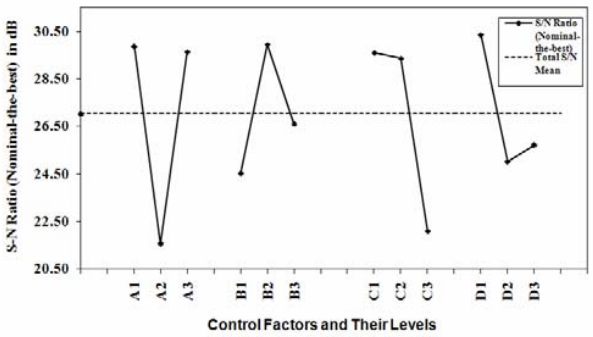

Fig. 2 S/N graph of threshold voltage for PMOS Device

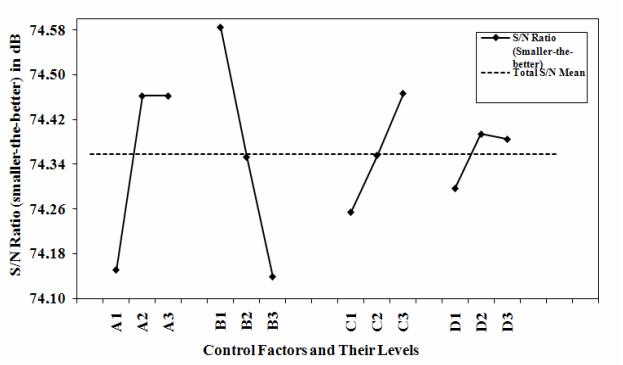

Fig. 3 S/N graph of leakage current for PMOS Device

C.Analysis of Variance (ANOVA)

The analysis of variance (ANOVA) is a common statistical technique to determine the percent contribution of each factor for results of the experiment. It is also can be used to investigate which of the process parameters significantly affect the performance characteristics [11]. It calculates parameters known as sum of squares (SS), degree of freedom (DF), variance, F-value and percentage of each factor. The SS is a measure of the deviation of the experimental data from the mean value of the data. The total sum of squares can be calculated as [7],[17]:

$$SS_T = \sum_{i=1}^{n} (\eta_i - m)^2 \quad (5)$$

where n is the number of experiments in the orthogonal array, η_i is the mean S/N ratio for the *i*th experiment and *m* is the average of the nine η_i values. Similarly the SS for each factor is sum of the square of average performance of a factor at each level, given by [7]

$$SS_{p(A)} = 3\left[(mA_1 - m)^2 + (mA_2 - m)^2 + (mA_3 - m)^2\right] \quad (6)$$

$$SS_{p(B)} = 3\left[(mB_1 - m)^2 + (mB_2 - m)^2 + (mB_3 - m)^2\right] \quad (7)$$

$$SS_{p(C)} = 3\left[(mC_1 - m)^2 + (mC_2 - m)^2 + (mC_3 - m)^2\right] \quad (8)$$

$$SS_{p(D)} = 3\left[(mD_1 - m)^2 + (mD_2 - m)^2 + (mD_3 - m)^2\right] \quad (9)$$

The degrees of freedom of the tested process parameter DF=t-1, where *t* the repetition of each level of the process parameter, *p*. DF rather than the number of observation is used in the variance calculation. The variance (mean square) of the process parameter tested is $V_p = \frac{SS_p}{DF}$ [7],[10]. F-value for each process parameter is the ratio of variance due to the effect of a factor and variance due to the error term, $F_p = \frac{V_p}{V_e}$. It is used to measure the significance of the factor under investigation with respect to the variance of all the factors included in the error term. Usually the larger the F-value, the effect on the performance characteristic is greater due to the change of the process parameter [17]. The percent contribution of each factor is the ratio of the factor sum to the total expressed in percent. For example, the percentage contribution ρ due to factor A can be calculated as [7]:

$$\rho_A = \frac{SS_{p(A)}}{SS_T} \times 100 \quad (10)$$

When the variance of the error is zero, the F-value for factors A, B, C and D is undetermined. Then the variance of the error can be combined with another smallest factor variance to calculate a new error variance which can be used to produce meaningful results. The process of disregarding an individual factor's contribution and then subsequently adjusting the contribution of the other factor is known as pooling.

The results of ANOVA for the PMOS device are shown in Table IX. According to these analyses, factor A (halo implant dose) was found to be the major factor affecting the threshold voltage (40%), whereas factor B (S/D implant dose) was the major factor affecting the leakage current (52%). The percent factor effect on S/N Ratio indicates the priority of a factor (process parameter) to reduce variation. For a factor with a high percent contribution and a small variance (mean square) will have a great influence on the performance.

TABLE IX
RESULTS OF ANOVA FOR VTH AND ILEAK IN PMOS DEVICE

Response	Process Parameter	DF	SS	Mean square	F-Value	Factor Effect on SNR (%)
V_{TH}	Halo Implant Dose	2	134	67	20	40
	S/D Implant Dose	2	45	23	7	13
	Oxide Growth Temp	2	109	55	16	32
	Silicide Anneal Temp	2	51	25	8	15
I_{LEAK}	Halo Implant Dose	2	0	0	17	34
	S/D Implant Dose	2	0	0	26	52
	Oxide Growth Temp	2	0	0	6	12
	Silicide Anneal Temp	2	0	0	2	3

In this research, factor C (oxide growth temperature) and factor A (halo implant dose) were found to be the second ranking factor affecting the threshold voltage (32%) and leakage current (34%) respectively. The analysis of average performance showed that the optimum condition is $A_1B_1C_1$. Because factor D (silicide anneal temperature) was found not significant (pooled) in leakage current, it could be set at any level [7]. The full recommendation for optimization is $A_1B_1C_1D_1$.

D.Confirmation of Optimum Run

The confirmation experiment is the final step in the first interaction of the design of the experiment process. The purpose of the confirmation experiment is to validate the conclusions drawn during the analysis phase[17]. Best setting of the process parameters for PMOS device that effects on V_{TH} and I_{Leak} , which had been suggested by Taguchi method is shown in Table X.

TABLE X
BEST SETTING OF THE PROCESS PARAMETERS

Symbol	Process Parameters	Unit	Best Value
A	Halo Implantation Dose	atom cm^{-3}	3.36E13
B	S/D Implantation Dose	atom cm^{-3}	6.55E13
C	Oxide Growth Temperature	^oC	815
D	Silicide Anneal Temperature	^oC	900

Once the optimal level of the process parameters is selected, the final step is to predict and verify the improvement of the performance characteristic using the optimal level of the process parameters. The results of the final simulation for both parameters, V_{TH} and I_{Leak} are shown in Tables XI and XII.

TABLE XI
RESULTS OF THE CONFIRMATION EXPERIMENT FOR VTH

Threshold Voltage (Volts)				S/N Ratio
$V_{TH}1$	$V_{TH}2$	$V_{TH}3$	$V_{TH}4$	(Nominal-the-Best)
-0.1518	-0.1582	-0.1565	-0.1596	33.30

TABLE XII
RESULTS OF THE CONFIRMATION EXPERIMENT FOR ILEAK

Leakage Current (mA/μm)				S/N Ratio
$I_{Leak}1$	$I_{Leak}2$	$I_{Leak}3$	$I_{Leak}4$	(Smaller-the-Best)
0.192	0.196	0.196	0.195	74.21

The S/N ratios for V_{TH} and I_{leak} after the optimization approaches are 33.30 dB and 74.21 dB respectively. Both values are closer and within the predicted value. For V_{TH}, 33.3 dB is closer to the predicted range S/N ratio of 32.99 to 32.83 dB (32.91 ± 0.08 dB). While for I_{Leak}, 74.21 dB is within predicted range S/N ratio 74.50 to 74.05 dB (74.27 ± 0.23 dB). These show that Taguchi Method can predict the optimum solution in finding the 45nm PMOS fabrication recipe with appropriate threshold voltage and leakage current values. The threshold voltage and leakage current for PMOS device after optimization approaches are -0.157V at I_{Leak}=0.195mA/μm respectively. These values are exactly same with International Technology Roadmap for Semiconductor (ITRS) prediction [15].

IV. CONCLUSION

As the conclusion, the optimum solution in achieving the desired transistor was successfully predicted by using Taguchi Method. Threshold voltage (V_{TH}) is the main response in determining whether the device works or not. Leakage current should also be kept as low as possible to increase the speed of the device by shortening the time to accumulate charge in the channel for a transistor to turn on. In this research, halo implant dose and oxide growth temperature are the most effective parameters with respect to the threshold voltage, whereas S/D implant dose is the most effective parameter that has the strongest effect on the leakage current for this device

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