International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:2, No:9, 2008

Design of Folded Cascode OTA in Different Regions of Operation through g_m/I_D Methodology

H. Daoud Dammak, S. Bensalem, S. Zouari, and M. Loulou

***Abstract*—**This paper presents an optimized methodology to folded cascode operational transconductance amplifier (OTA) design. The design is done in different regions of operation, weak inversion, strong inversion and moderate inversion using the g_m/I_D methodology in order to optimize MOS transistor sizing.

Using 0.35µm CMOS process, the designed folded cascode OTA achieves a DC gain of 77.5dB and a unity-gain frequency of 430MHz in strong inversion mode. In moderate inversion mode, it has a 92dB DC gain and provides a gain bandwidth product of around 69MHz. The OTA circuit has a DC gain of 75.5dB and unity-gain frequency limited to 19.14MHZ in weak inversion region.

***Keywords*—**CMOS IC design, Folded Cascode OTA, g_m/I_D methodology, optimization.

I. Introduction

THE evolution of the microelectronics industry is distinguished by the raising level of integration and complexity. It aims to decrease exponentially the minimum feature sizes used to design integrated circuits. The cost of design is a great problem to the continuation of this evolution. Senior designer's knowledge and skills are required to ensure a good analogue integrated circuit design. To fulfill the given requirements, the designer must choose the suitable circuit architecture, although different tools partially automating the topology synthesis appeared in the past [1]-[4].

The optimization becomes an important method; a heuristic process was developed in [5]. Nominal circuits design was considered in [6]-[7], sizing problems were discussed in [8]-[10], and worst-case optimization in [11]-[13]. Several optimization tools were developed, such as equation based GPCAD [14]-[15], AMG using a symbolic simulator and the simulation based ASTRX/OBLX [16]-[18]. Recently, the sizing problem from different aspects are addressed in numerous papers ([13], [19]-[24]).

Designing high-performance base band analog circuits is still a hard task toward reduced supply voltages and increased frequency. Current tendency focus on some radio-software receivers which suppose a RF signal conversion just after the antenna. Thus, a very higher sampling frequency and resolution analog-to-digital converter design is required. The OTA is a basic element in this type of circuit whether switched capacitors technique is kept for ADC design.

Our target was to design a folded cascode OTA circuit in sight of Sigma Delta analog-to-digital converter design using for wide band radio applications.

This paper is organized as follows. Folded cascode OTA structure is analyzed in section II. Section III presents the OTA circuit design in the three regions of operation. Section IV gives design window. Finally some concluding remarks are provided after evaluating our study toward other works.

H. Daoud Dammak, S. Bensalem, S. Zouari and M. Loulou are with the national National School of Engineering of Sfax, B.P. 3038, Sfax, Tunisia (e-mails: daoud.houda@tunet.tn, samir.bensalem@isecs.rnu.tn, zouari@enis.rnu.tn, mourad.loulou@ieee.org).

II. Folded Ota Structure

A. NMOS Input Transistor

The input stage provides the gain of the operational amplifier. Due to the greater mobility of NMOS device, PMOS input differential pair presents a lower transconductance than carrier a NMOS pair. Thus, NMOS transistor has been chosen to ensure the largest gain required.

B. Architecture Analysis

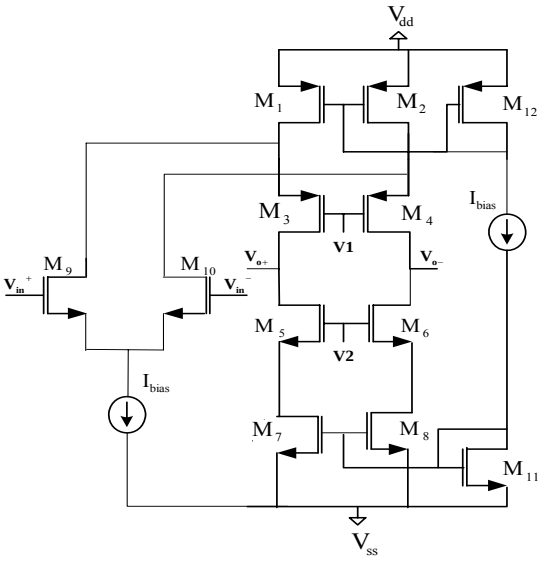

Fig. 1 Folded cascode OTA topology

The main bottleneck in an analog circuit is the operational amplifier. Different types of OTA configuration are available to the designer who tend to improve performances

requirements design [25]. We opt for a "folded cascode" op-amp due to its large gain and high bandwidth performances. Fig. 1 presents the folded cascode OTA (the name "folded cascode" comes from folding down p-channel cascode active loads of a diff-pair and changing the Mosfets to n-channels).

To understand the operation of the folded cascode OTA, this last has a differential stage consisting of NMOS transistors M_9 and M_{10}. Mosfets M_{11} and M_{12} provide the DC bias voltages to M_1-M_2-M_7-M_8 transistors. The open-loop voltage gain and gain bandwidth are given by (1) and (2) below:

$$A_V = \frac{g_{m9} \cdot g_{m6} \cdot g_{m4}}{I_D^2 \left(g_{m4} \lambda_N^2 + g_{m6} \lambda_P^2 \right)} \quad (1)$$

$$GBW = \frac{g_{m9}}{I_D} \frac{I_D}{C_L} \quad (2)$$

Where, g_{m4}, g_{m6} and g_{m9} are respectively the transconductances of transistors M_4, M_6 and M_9. I_D is the bias current flowing in Mosfets M_4, M_6, and M_9. C_L is the capacitance at the output node, λ_N and λ_P are the parameters related to channel length modulation respectively for NMOS and PMOS devices. Taking into account the complementarity between the transistors M_4 and M_6:

$$g_{m4} = g_{m6} \quad (3)$$

The gain expression becomes:

$$A_V = \frac{g_{m9} \cdot g_{m6}}{I_D^2 \left(\lambda_N^2 + \lambda_P^2 \right)} \quad (4)$$

III. Folded Cascode OTA Design

The op-amp is characterized by various performances like open-loop voltage gain, unity-gain bandwidth, slew rate, noise and so on. These performances measures are fixed by the design parameters, e.g., transistor sizing, bias currents, and other component values [26].

The aim of this work is to determine values of the design parameters that optimize an objective feature whereas satisfying specifications or constraints. In this paper, we introduce the design of the folded cascode OTA amplifier in the three regions of operation. This design applies a synthesis procedure based on the g_m/I_D methodology introduced by Flandre and Silveira [27].

A Sizing Algorithm

The formulation of a design flow clarifies a top-down synthesis methodology for CMOS OTA architectures (Fig.2) [28]. In fact, this last starts by fixing the specifications to optimize for example: gain and unity gain frequency in order to determine the unknowns that are MOS device sizes and bias current:

- Equation (2) directly yields g_{m9} from the given transition frequency and capacitive load, whereas g_{m9}/I_D is derived from the specified DC open-loop gain and the chosen technology using equation (4).
- g_{m9} and g_{m9}/I_D yield the bias current I_D and furthermore g_{m9}/I_D gives I' where I'= $I_D/(W/L)$.
- W/L is finally given by I_D/I'.

The universal g_m/I_D as a function of $I_D/(W/L)$ characteristic of the CMOS technology under consideration (0.35µm of AMS) is exploited in order to apply the method quoted previously and compute the design parameters (Fig. 3). This characteristic is obtained by simulation and defined in the three regions of operation of transistor.

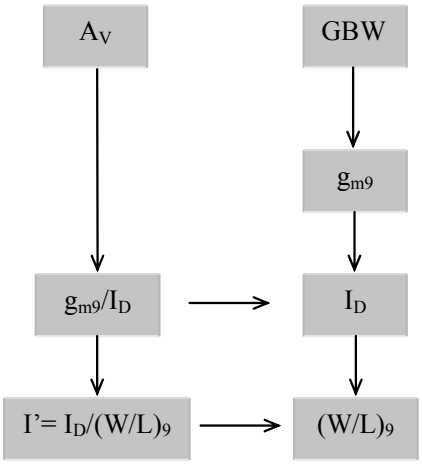

Fig. 2 Design flow

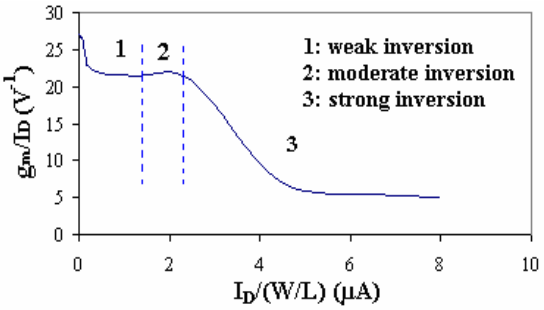

Fig. 3 g_m/I_D as a function of $I_D/(W/L)$

B. Weak Inversion Region

The operating range of transistors can be entirely exploited: weak, moderate or strong inversion, linear or saturated mode, quasi-static or high-frequency operation [30].

The transistors are traditionally biased in the saturation mode in analogue circuits. But, they can be operated in strong inversion or weak inversion. Transistors biasing in weak inversion provide higher transconductance and supply a larger gain with a smaller current. These transistors present a low thermal noise. In our design, we will study the folded cascode OTA behaviour in the three regions of operation.

C. Design in Weak Inversion

As shown in Fig. 4, we note that weak inversion presents higher g_m/I_D values with smaller current, so an increased gain is favorable for this operating mode.

We set specifications to the circuit of Fig. 1 presented by Table I.

TABLE I
SPECIFICATIONS

Specifications	Values
A_v (dB)	105
GBW (MHz)	21.5
C_L (fF)	10
V_{dd}/V_{ss} (V)	±1
Channel length (µm)	1

After applying the design strategy clarified previously, we obtain the parameters computed and summarized in Table II.

TABLE II
DESIGN PARAMETERS IN WEAK INVERSION

Parameters	Values
I_D (nA)	50
$W_{9,10}$ (µm)	3.5
$W_{3,4}$ (µm)	2.7
$W_{5,6,7,8}$ (µm)	1
$W_{1,2,12}$ (µm)	5.4
W_{11} (µm)	2
$V_1 = V_2$ (mV)	-428

The designed folded cascode OTA is biased at ±1V power supply voltage using CMOS technology of 0.35 µm of AMS with the BSIM3V3 MOSFET model. The circuit denotes an offset voltage of 0.4mV, a Slew Rate of 3.3V/µs, a wide input common-mode range of [-0.99V, 0.98V], a wide output common-mode range between -0.96V and 0.95V. It consumes 0.6µW.

Moreover, our device is able to achieve a degrading gain of 75.5dB, a bandwidth of 19.14MHz with phase margin of 67degrees (Fig. 4), a good common mode rejection ratio of 126.8dB and a low transconductance of 1.8µS kept constant for a wide range of frequency (Fig. 5).

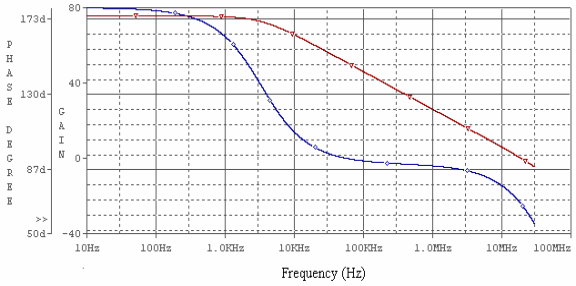

Fig. 4 Gain and phase curve

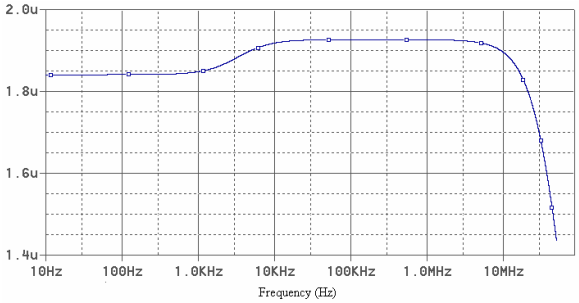

Fig. 5 OTA's transconductance in weak inversion region

D. Design in Moderate Inversion

In weak inversion, we succeed in reaching good performances with very low consumption; hence, the gain bandwidth product isn't raised and necessary enough to satisfy wide band applications.

In order to improve this parameter, relatively with the same lower consumption, we will study the design of the OTA in moderate inversion region. Thus, we propose specifications illustrated by Table III that put more constraints on OTA gain bandwidth product.

TABLE III
SPECIFICATIONS

Specifications	Values
A_v (dB)	100
GBW (MHz)	70
C_L (pF)	0.1
V_{dd}/V_{ss} (V)	±2
Channel length (µm)	1

Likewise, the design strategy described in section A is adopted keeping small signals model invariant in different operation's regions of transistor. The design parameters found are collected in Table IV. The voltages V_1 and V_2 are well fixed at -256mV.

TABLE IV
DESIGN PARAMETERS IN MODERATE INVERSION

Parameters	Values
I_D (µA)	2
$W_{9,10}$ (µm)	9
$W_{3,4}$ (µm)	2.7
$W_{5,6,7,8}$ (µm)	1
$W_{1,2,12}$ (µm)	5.4
W_{11} (µm)	2
$V_1 = V_2$ (mV)	-256

The OTA circuit can reach a DC gain of 92dB, a unity-gain frequency of 69MHz with phase margin of 74.5degres (Fig. 6). Its transconductance is about 65µS (Fig. 7). It dissipates 48µW.

In this behaviour mode, the gain and GBW characteristics are interesting, also a wide input and output swings are maintained.

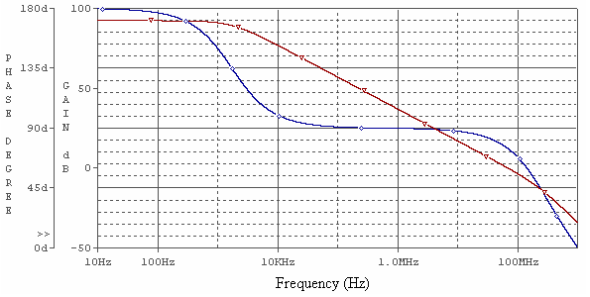

Fig. 6 Gain and phase curve

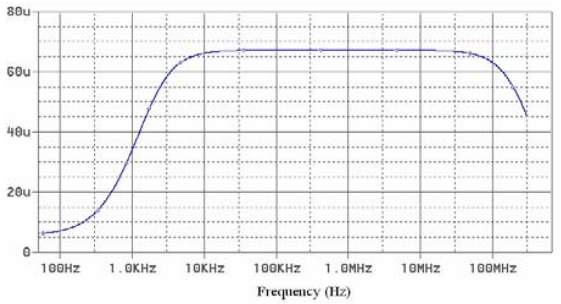

Fig. 7 OTA's transconductance in moderate inversion region

E. Design in Strong Inversion

In weak inversion and for bias current relatively considerable, we estimate reaching bandwidths satisfying wide band applications requirements.

We remark that g_m/I_D ratio decreased as a function of current in this region of operation. Then, we fixed specifications given by Table V.

TABLE V
SPECIFICATIONS

Caractéristiques	Valeurs
A_v (dB)	80
GBW (MHz)	450
C_L (pF)	0.1
V_{dd}/V_{ss} (V)	±2
Channel length (µm)	1

The Mosfets sizes are computed as a result of the design flow (Table VI). We conclude that the sizes found in strong inversion are more important than those obtained in weak and moderate inversion; this can be explained by the use of high current towards other regions.

TABLE VI
DESIGN PARAMETERS IN STRONG INVERSION

Parameters	Values
I_D (µA)	27.5
$W_{9,10}$ (µm)	14
$W_{3,4}$ (µm)	5.4
$W_{5,6,7,8}$ (µm)	2
$W_{1,2,12}$ (µm)	10.8
W_{11} (µm)	4
$V_1 = V_2$ (mV)	-318

The folded cascode OTA has a gain of 77.5dB, a large unity-gain frequency of 430MHz and a phase margin of 58.2degrees. Its transconductance is about 396µS (Fig. 8).

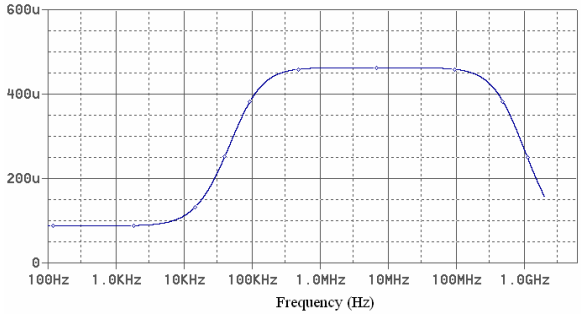

Fig. 8 OTA's transconductance in strong inversion region

Several characteristics were depicted in folded cascode OTA designing step (Table VII). This topology works in various frequency ranges. According to the application and its constraints, we choose the mode of operation of transistors.

IV. Design Window

To verify some design parameters namely unity gain frequency and drain source current, we try to present a design window in different regions of operation that yields a different couple of (F_t, I_D) values, using MATLAB tool.

As illustrated in Fig. 9 and Fig. 10, in strong inversion, a drain current of 27.5µA leads to a unity-gain frequency of 460MHz. In moderate inversion, for a current fixed at 2µA, GBW value is around 90MHz.

We notice that unity gain frequency increases in moderate inversion region, so we have to take the change of small signals model in moderate inversion into account.

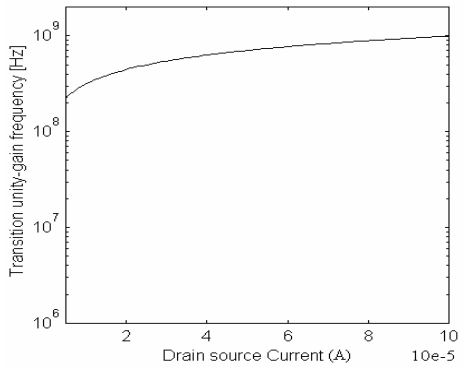

Fig. 9 Unity gain frequency as a function of drain source current in strong inversion region

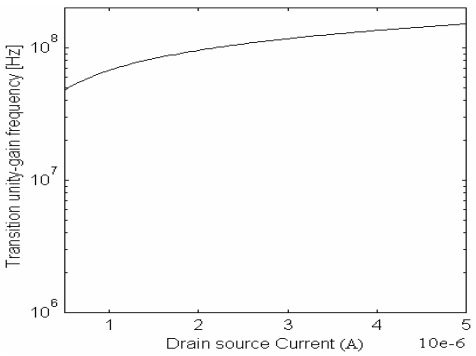

Fig. 10 Unity gain frequency as a function of drain source current in moderate inversion region

V. Comparison of Results

After discussing the different parameters of OTA design we can evaluate our study toward other works. The performance of the folded cascode OTA from this work has been compared to two recent OTA circuits design. The first is a Class-AB OTA [29]. The second was a telescopic OTA architecture presented in [30]. This comparison is given in Table VIII. It is

clearly seen that with folded cascode OTA architecture, we reach low power low voltage topology with high static gain.

VI. Conclusion

Consequently, the synthesis of high-performance analog integrated circuits constitutes a complex activity requiring the command of many concepts. As a result, the analog designer remains a rare and highly-valued engineer worldwide.

This contribution presents the strategy design of folded cascode OTA in the three operation's modes of transistor: weak inversion, strong inversion and moderate inversion, so, the goal to reach high gain and large bandwidth has been fulfilled.

We estimate that g_m/I_D methodology is well adopted for sizing in different function modes to reach extremely performances offered by a given technology.

Future work would involve the exploitation of these results on folded cascode OTA for low consumption and wide band applications to use it in wide band analog-to-digital converters.

TABLE VII
Folded Cascode OTA Specifications

Specifications	Weak inversion	Moderate inversion	Strong inversion
DC Gain (dB)	75.57	92	77.53
GBW (MHz)	19.14	69	430
Transconductance (µS)	1.8	65	396
Phase margin (degrees)	67	74.5	58
Offset voltage (µV)	430.4	246	337
Output swing (V)	[-0.96 ; 0.95]	[-1.94 ; 1.84]	[-1.84 ; 1.72]
Input swing (V)	[-0.99 ; 0.98]	[-1.95 ; 1.87]	[-1.95 ; 1.87]
Slew Rate (V/µs)	3.3	16.5	196
CMRR (dB)	126.8	133	114
PSRR p, n (dB)	18	45.7	46.5
Supply voltage (V)	±1	±2	±2
Bias current (µA)	0.1	4	55
Power consumption (µW)	0.6	48	660

TABLE VIII
Performances Comparison

Performance/Design	Yao & Steyaert [29]	Craig Brendan Keogh [30]	This work
OTA Architecture	Class-AB	Telescopic	Folded cascode
Technology (µm)	0.09	0.18	0.35
DC Gain (dB)	50	79	75.57
GBW (MHz)	57	8.5	19.14
Phase margin (degrees)	57	78	67
Supply voltage (V)	1	0.925	1
Power consumption (µW)	80	4.6	0.6

REFERENCES

[1] M.G.R. Degrauwe et al.., "IDAC: An interactive design tool for analog CMOS circuits," IEEE J.Solid-State circuits, vol. sc-22, no. 6, dec.(1987), pp. 1106-1116.
[2] R.Harjani, R.A. Rutenbar and L.R. Carley, "OASYS: A framework for analog circuit synthesis," IEEE Trans. Computer-Aided Design, vol. 8, no. 12, Dec. (1989), pp. 1247-1266.
[3] H. Y. Koh, C.H Séquin and P.R. Gray, "OPASYN: A compiler for CMOS operational amplifiers," IEEE Trans. Computer-Aided Design, vol. 8, no. 12, Dec. (1990), pp. 113-125.
[4] J.P. Harvey, M.I. Elmasry and B. Leung, "STAIC: An interactive framework for synthesizing CMOS band BiCMOS analog circuits," IEEE Trans.Computer-Aided Design, vol. 11, no. 11, Nov. (1992), pp. 1402-1417.
[5] M. Fakhfakh, M. Loulou, and N. Masmoudi, "Optimizing performances of switched current memory cells through a heuristic," Journal of Analog Integrated Circuits and Signal Processing, Springer Editor, (2006).
[6] R.K. Brayton, G.D. Hachtel and A.L. Sangiovanni-Vincentelli, "A survey of optimization techniques for integrated-circuit design," Proc. IEEE, vol. 69, no. 10, Oct. 1981, pp. 1334-1364.
[7] W. Nye et al.., "DELIGHT.SPICE: An optimization–based system for the design of integrated circuits,"IEEE Trans.Computer-Aided Design, vol. 7, no. 4, Apr. (1988), pp. 501-519.
[8] S.W. Director and G.D. Hachtel, "The simplicial approximation approach to design centering,"IEEE Trans. Circuits Syst. I, vol. Cas-29, no. 2, Feb. (1982),pp. 88-96
[9] K.J.Antreich and R.K Koblitz, "Design centering by yield prediction," IEEE Trans. Circuits Syst. I, vol. Cas-29, no. 2, Feb. (1982), pp. 88-96.
[10] P. Feldmannand S. W. Director," Integrated circuit quality optimization using surface integrals ," IEEE Trans. Computer-Aided Design vol. 12, no. 12,Dec. 1993; pp. (1868-1879).
[11] K.J.Antreich, H.E. Hraeb and C.U. Wieser," Circuit analysis and optimization driven by worst-case distances," IEEE Trans. Computer-Aided Design vol. 13, no. 1, Jan. (1994), pp. 57-71.
[12] A. Dharchoudhury and S.M. Kang, "Worst-case analysis and optimization of VLSI circuit performances," IEEE Trans. Computer-Aided Design vol. 14, no. 4,Apr. (1995), pp. 481-492.
[13] A. Burmen et al.., "Automated robust design and optimization of integrated circuits by means of penalty functions," int. J. Electron. Comm.,57, no. 1, (2003), pp. 47-56.
[14] M. del Mar Hershenson, S.P. Boyd and T.H. Lee, "GPCAD: A tool for CMOS op-amp synthesis," 1998 IEEE/ACM Int. Conf.Comput-Aided Design, New York, (1998), pp. 296-303.
[15] M. del Mar Hershenson, S.P. Boyd and T.H. Lee, "Optimal design of a CMOS op-amp via geometric programming," IEEE Trans. Computer-Aided Design vol. 20, no. 1, Jan. (2001), pp. 1-21.
[16] G. Gielen at al..,"An analogue module generator for mixed analogue/digital ASIC design," Int. J.Circuit theory and App.,vol. 23, no. 4, July-Aug. (1995),pp.269-283.
[17] G.G.E. Gielen, H.C.C. Walscharts and W.M.C. Sansen," Analog circuit design optimization based on symbolic simulation and simulated annealing," IEEE J. Solid-State circuits, vol. 25, no. 3 June (1990), pp. 707-713.
[18] E.S.Ochotta, R.A. Rutenbar and L.R. Carley, "Sunthesis of high-performances analog circuits in ASTRX/OBLX,"IEEE Trans. Computer-Aided Design vol. 15, no. 3, Mar. (1996), pp. 273-294.
[19] G. Debyser and G. Gielen, "Efficient analog circuit synthesis with simultaneous yield and robustness optimization," 1998 IEEE/ACM, Int. Conf. Computer-Aided Design, New York, (1998), pp. 308-311.
[20] R. Schwencker et al.., "Automating the sizing of analog CMOS circuits by consideration of structural constraints," DATE Conf. And Exhibition, 1999, Los Alamitos, (1999), pp. 323-327.
[21] R. Phelps et al., "Anaconda: simulation-based synthesis of analog circuitsvia stochastic pattern search," IEEE Trans. Computer-Aided Design vol. 19, no. 6, June (2000), pp. 703-717.
[22] T. Mukherjee, L.R. Carley and R.A Rutenbar, "Efficient handling of operating range and manufacturing line variations in analog cell synthesis," IEEE Trans. Computer-Aided Design vol. 19, no. 8, Aug. (2000), pp. 825-839.
[23] F. Schenkel et al., "Mismatch analysis and direct yield optimization by spec-wise linearization and feasibility-guided search," Proc. 38th DAC, New York, (2001), pp. 22-38.
[24] P. Mandal and V. Visvanthan, "CMOS op-amp sizing using a geometric programming formulation," IEEE Trans. Computer-Aided Design vol. 20, no. 1, Jan. (2001), pp. 22-38.
[25] Behzad Razavi, "Design of Analog CMOS Integrated Circuit", TheMcGraw-Hill Companies, Inc., United States, (2001), ISBN:0-07-118815-0.
[26] M. Loulou, S. Ait Ali and N. Masmoudi, "Conception et Optimisation d'un Amplificateur Opérationnel Rail to Rail CMOS Faible Tension Faible Consommation" Journal Scientifique Libannais, le Conseil National de la Recherche Scientifique- Liban Vol. 4, N°.1, (2003), pp. 75-90.
[27] Silveira, D. Flandre et P.G.A. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and application to the synthesis of a SOI micropower OTA", IEEE J. of Solid State Circuits, vol. 31, n. 9, sept. (1996).
[28] M. Banu, J. M. Khoury, and Y. Tsividis, "Fully Differential Operational Amplifier with Accurate Output Balancing," IEEE Journal of Solid State circuits, Vol. 23, No. 6, pp. December (1990).
[29] Y. Libin, M. Steyaert, and W. Sansen, "A 1–V 140-μW 88-dB Audio Sigma-Delta Modulator in 90-nm CMOS", IEEE Journal of Solid State circuit, Vol. 39, NO. 11, November (2004).
[30] Craig Brendan Keogh, "Low-Power Multi-Bit ΣΔ–Modulator Design for portable Audio Application", Stockholm, March (2005).

Houda Daoud Dammak was born in Sfax, Tunisia in 1980. He received the Electrical Engineering Diploma then the Master degree in electronics from the National School of Engineering of Sfax "ENIS", respectively, in 2004 and 2005. He joints the Electronic and Information Technology Laboratory of Sfax "LETI" since 2004 and he has been a PhD student at the National School of Engineering of Sfax "ENIS" from 2005. His current research interests are on analogue CMOS integrated circuits design.

Mourad Loulou was born in Sfax, Tunisia in 1968. He received the Engineering Diploma from the National School of Engineering of Sfax in 1993. He received his Ph.D. degree in 1998 in electronics system design from the University of Bordeaux France. He joints the electronic and information technology laboratory of Sfax "LETI" since 1998 and he has been assistant Professor at the National School of Engineering of Sfax from 1999. Since 2004 he has been an associate Professor at the same institution. Actually he supervises the Analogue and Mixed Mode Design Group of LETI Laboratory. His current research interests are on analogue, mixed and RF CMOS integrated circuits design and automation.

Samir Ben Salem was born in 1976 in Sfax, Tunisia. He received the electrical engineering degree in 2002 and Master degree on electronics and communication in 2003, both from the National School of Engineering of Sfax (ENIS), Tunisia. He is currently working toward the Ph.D. degree in Electronic at the same school. His research interest is to design RF integrated circuit for wireless communication transceivers, especially the design of active RF oscillator and filter for front end receiver.