International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:3, No:2, 2009

# Harmonic Reduction In Three-Phase Parallel Connected Inverter

*M.A.A. Younis, N. A. Rahim, and S. Mekhilef*
Dept. of Electrical Engineering, University of Malaya, Kuala Lumpur, Malaysia.

***Abstract*—** This paper presents the design and analysis of a parallel connected inverter configuration of. The configuration consists of parallel connected three-phase dc/ac inverter. Series resistors added to the inverter output to maintain same current in each inverter of the two parallel inverters, and to reduce the circulating current in the parallel inverters to the minimum. High frequency third harmonic injection PWM (THIPWM) employed to reduce the total harmonic distortion and to make maximum use of the voltage source. DSP was used to generate the THIPWM and the control algorithm for the converter. Selected experimental results have been shown to validate the proposed system.

Keywords: *Three-phase inverter, Third harmonic injection PWM, inverters parallel connection.*

## I. INTRODUCTION

Improvements in fast switching power devices have led to an increased interest in voltage source inverters (VSI) with pulse width modulation control (PWM). Control methods which generate the necessary PWM patterns could be classified as voltage controlled and current controlled PWM.

With PWM control technologies, ac side of the three-phase inverter has the abilities of controllable power factor, sinusoidal output currents and bi-directional power transfer [1] [2]. The third harmonic injection method to control the power factor of the inverter output current used for three-phase inverter. However, it is very difficult to generate the right third harmonic amplitude [3] [4]. In hysteresis control the switching frequency varies significantly according to the power level and the dc link [5] [6].

## II. THREE PHASE INVERTER

A standard three-phase inverter is shown in Figure 1 consisting of six controlled switches such as IGBT. In this converter, the line currents can be shaped to be sinusoidal at a unity power factor, as well as the output ac voltage can be regulated at a desired value. The inverter is connected to the load through three LC filters. THIPWM employed to make full use of the DC bus voltage with minimum harmonic distortion in the output voltage and current.

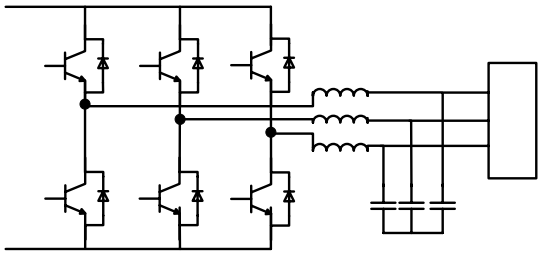

Figure 1: Three-Phase Inverter

The modulating signal is generated by injecting the third harmonic component to the 50 Hz fundamental component as given in the following equations.

$$V_{ra} = 1.15\sin\omega t + 0.19\sin 3\omega t \quad (1)$$

$$V_{rb} = 1.15\sin\left(\omega t - \frac{2}{3}\pi\right) + 0.19\sin 3\omega t \quad (2)$$

$$V_{rc} = 1.15\sin\left(\omega t - \frac{4}{3}\pi\right) + 0.19\sin 3\omega t \quad (3)$$

Using the modulator given will maintain the peak voltage equal to the dc voltage.

The SIMULINK Embedded Target for the TI C2000 blocks used to construct system models and real-time control algorithm which is used from the SIMULINK library. Target for TI C2000 used along with Link for Code Composer Studio to automate code generation, execution, and communication with TI evaluation boards by inserting blocks for optimized functions, together with the appropriate board peripherals, into the model [8]. Three ePWM blocks used to obtain three-phase THIPWM for the three-phase inverter. Each ePWM block generate switching signal for one leg of the inverter as shown in Figure 2.

The modulating signal data generated using equation 1, 2 and 3 and saved in lookup table. The carrier is provided by the ePWM block by applying suitable PWM setting. The carrier frequency is calculated from the following equations when the counter setting is up/down.

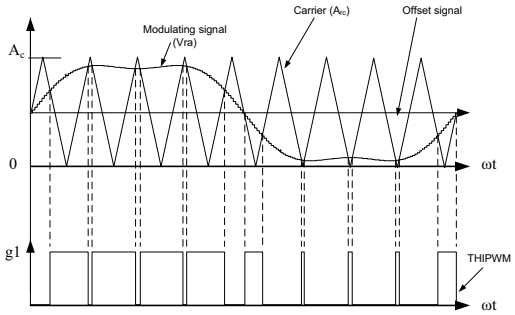


Figure 2: Generation of THIPWM

$$TPWM = 2(TBPRD \times TTBCLK) \quad (4)$$

$$FPWM = \frac{1}{TPWM} \quad (5)$$

$$TBCLK = \frac{SYSCLKOUT}{HSPCLKDIV \times CLKDIV} \quad (6)$$

Where TPWM is the PWM interval, TBRD is the value saved in TBPRD register, TTBCLK is the time of one clock cycle, and FPWM is the carrier frequency. The clock frequency is calculated using equation 4 where SYSCLKOUT is the synchronous clock frequency which 100MHz, HSPCLKDIV is High Speed Time-base Clock Prescale Bits which to be selected as one of the following values (1, 2, 4, 6, 8, 10, 12, or 14). CLKDIV is Time base Clock Prescale Bits which to be selected as one of the following values (2, 2, 4, 16, 32, 64, or 128). The PWM cycle (TPWM) shown in Figure 3.

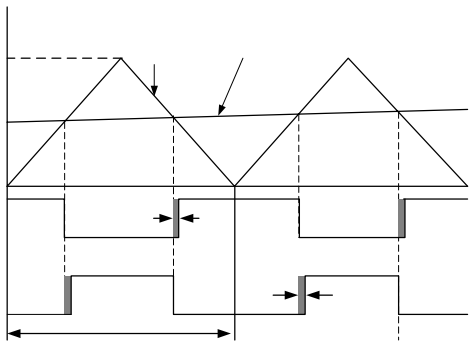

Figure 3: One Switching Interval

To prevent a short circuit in the dc link of IGBT voltage source PWM converters, the dead time period during which both the upper and lower IGBT's of the inverter phase leg are off, need to be inserted in switching signals. The dead time can cause waveform distortion and the fundamental voltage loss of the converter. To create dead time for the switches on the same leg the dead band (DB) module is used. The DB module supports independent values for rising edge (RED) and falling edge (FED) delays. The amount of delay is programmed using the dead band rising edge (DBRED) and dead band falling edge (DBFED) memory-mapped registers. These are 10-bit registers and their value represents the number of TBCLK periods a signal edge is delayed by. The formulas to calculate FED and RED respectively are as follow [8]:

$$FED = DBFED \times TTBCLK \quad (7)$$

$$RED = DBRED \times TTBCLK \quad (8)$$

## III. PARALLEL CONNECTION

In parallel operation, two or more inverters are tied together to share the load. In this paper, a system of two units will be discussed for convenience. Figure 4 shows two inverters which are directly connected at input and output ends. The parallel connection done for the two bridges such that the dc side filters and the ac side filter are common for the two parallel inverters. Inverters with different ratings some times encountered to increase the power capability of the system, it is desirable to share the currents according to the rated power of each module. If the bridges inverter used non-identical IGBT's, current sharing and circulating current are to be considered.

To study the current sharing and circulating current one mode of operation is to be considered. Figure 5 shows the mode of operation when the current IdA+ flowing through Q1A and Q1B, however the current IdA- flowing back to the source through Q6A and Q6b. the Figure shows the current sharing between Q1A and Q1B with two series resistors included.

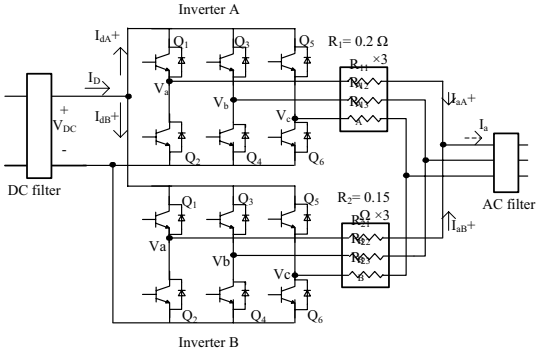


Figure 4: Parallel Connection of Two Three-Phase Inverters

The current sharing depends on the IGBT's Q1A and Q1B, If VCE1A not equal to VCE1B as a result IdA+ will not be equal to IdB+.

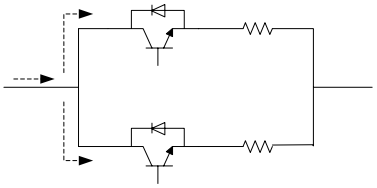

Figure 5: Circulating Current during One Switching Cycle

To maintain similar current sharing between the two inverters series resistor R1 and R2 added between each leg of the six

legs and the common point as shown in Figure 8. R1 box consists of three resistors R11, R12, and R13. Similarly R2 consists of R21, R22, and R23. Including the resistances R11A and R11B as shown in Figure 8 must satisfy the following condition:

$$V_{CE1A} + I_{dA}^{+} \cdot R_{11A} = V_{CE1B} + I_{dB}^{+} \cdot R_{11B} \quad (9)$$

*let*.

$$I_{dA}^{+} = I_{dB}^{+} = \frac{I_D}{2} \quad (10)$$

$$\frac{I_D}{2}\left(R_{11A} - R_{11B}\right) = V_{CE1B} - V_{CE1A} \quad (11)$$

$$or \qquad R_{11A} = \frac{2\left(V_{CE1B} - V_{CE1A}\right)}{I_D} + R_{11B} \quad (12)$$

To select the right value of R1 and R2 each of them suppose to be much smaller than the load resistance. The circuit will experience similar current sharing in all the modes of operation as a result the circulating current will be small.

## IV. Mode of Operation

The proposed configuration can be discussed in six modes of operation as shown in Table 4.1 considering the three-phase waveform shown in Figure 6. The modes of operation are discussed below:

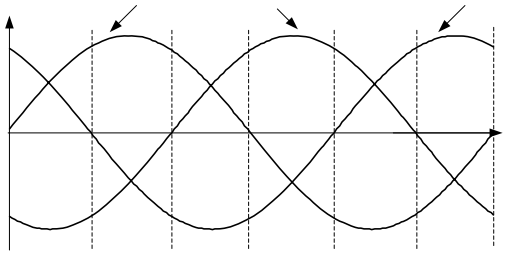

Figure 6: Three-phase waveform with six modes of operation

Table 1: The state of switches over 2π interval

| Mode | $Q_{1A}$, $Q_{1B}$ | $Q_{2A}$, $Q_{2B}$ | $Q_{3A}$, $Q_{3B}$ | $Q_{4A}$, $Q_{4B}$ | $Q_{5A}$, $Q_{5B}$ | $Q_{6A}$, $Q_{6B}$ |
|---|---|---|---|---|---|---|
| 1 | ON | OFF | OFF | ON | ON | OFF |
| 2 | ON | OFF | OFF | ON | OFF | ON |
| 3 | ON | OFF | ON | OFF | OFF | ON |
| 4 | OFF | ON | ON | OFF | OFF | ON |
| 5 | OFF | ON | ON | OFF | ON | OFF |
| 6 | OFF | ON | OFF | ON | ON | OFF |

*Mode1*

Phase a and phase c are in a positive cycle whereas phase b is in negative cycle. The DC voltage $V_{DC}$ applied to the inverter output through six switches $Q_{1A}$, $Q_{1B,}$ $Q_{4A}$, $Q_{4B,}$ $Q_{5A}$, and $Q_{5B}$ as shown in Figure 7.

*Mode 2*

Phase a is in a positive cycle whereas phase b and phase c are in the negative cycle. The DC voltage $V_{DC}$ applied to the inverter output through six switches $Q_{1A}$, $Q_{1B,}$ $Q_{4A}$, $Q_{4B,}$ $Q_{6A}$, and $Q_{6B}$ as shown in Figure 8.

*Mode 3*

Phase a and phase b are in a positive cycle whereas phase c is in negative cycle. The DC voltage $V_{DC}$ applied to the inverter output through six switches $Q_{1A}$, $Q_{1B,}$ $Q_{3A}$, $Q_{3B,}$ $Q_{6A}$, and $Q_{6B}$ as shown in Figure 9.

*Mode 4*

Phase a and phase c are in a negative cycle whereas phase b is in positive cycle. The DC voltage $V_{DC}$ applied to the inverter output through six switches $Q_{3A}$, $Q_{3B,}$ $Q_{2A}$, $Q_{2B,}$ $Q_{6A}$, and $Q_{6B}$ as shown in Figure 10.

*Mode 5*

Phase a is negative in a cycle whereas phase b and phase c are in positive cycle. The DC voltage $V_{DC}$ applied to the inverter output through six switches $Q_{3A}$, $Q_{3B,}$ $Q_{2A}$, $Q_{2B,}$ $Q_{5A}$, and $Q_{5B}$ as shown in Figure 11.

*Mode 6*

Phase a and phase b are in a negative cycle whereas phase c is in positive cycle. The DC voltage $V_{DC}$ applied to the inverter output through six switches $Q_{5A}$, $Q_{5B,}$ $Q_{2A}$, $Q_{2B,}$ $Q_{4A}$, and $Q_{4B}$ as shown in Figure 12.

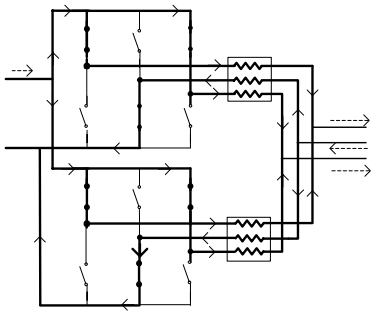

Figure 7: The current path during Mode 1

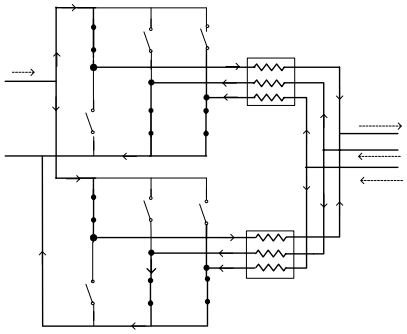

Figure 8: The current path during Mode 2.

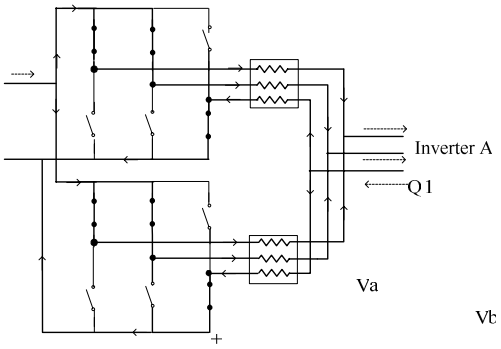


Figure 9: The current path during Mode 3.

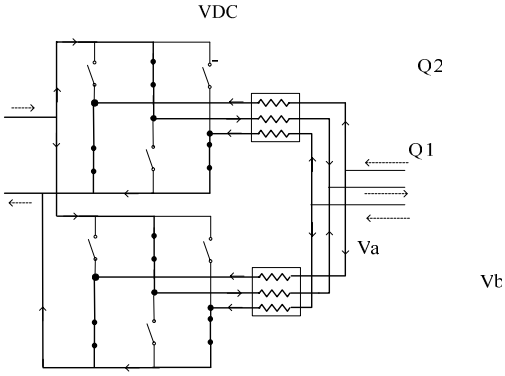


Figure 10: The current path during Mode 4

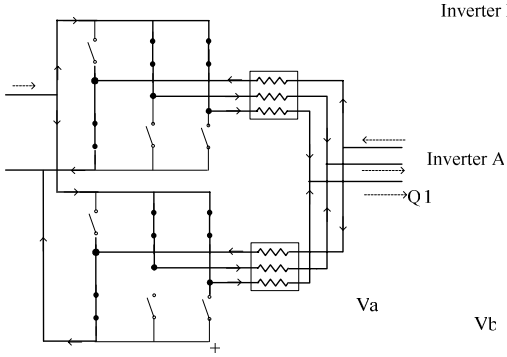


Figure 11: The current path during Mode 5.

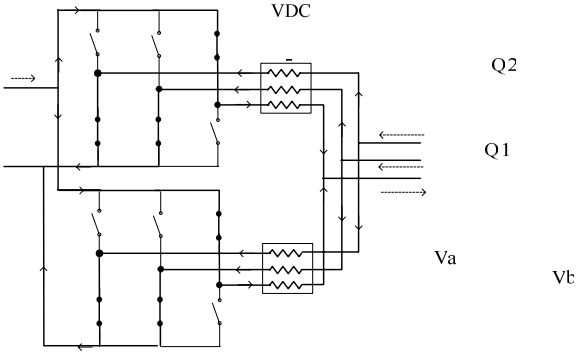


Figure 12: The current path during Mode 6.

## V. Efficiency of Parallel Connected Inverter

The power dissipation ($P_D$) and the efficiency (η) in the three-phase inverter can be calculated as follows:

$$P_D = P_{DC} - P_{AC} \quad (13)$$

$$\eta = \frac{P_{AC}}{P_{DC}} \quad (14)$$

Where $P_D$ is the power dissipation of the inverter, $P_{DC}$ is the DC source power, and $P_{AC}$ is the inverter output power. Assuming ripple free current on the DC source, and unity power factor on the AC side the input power and the output power are calculated as:

$$P_{DC} = I_{DC} \times V_{DC} \quad (15)$$

$$P_{AC,3\phi} = 3I_{ph} \times V_{ph} \quad (16)$$

The inverter power is mainly dissipated by the IGBTs. The parallel connection improves the switch power dissipation which improves the inverter efficiency.

## VI. Result and Discussion

A parallel connected inverter system was designed and implemented to verify the above discussion. The parameters of the system are as follow.

IGBT for inverter a is SSG60N60 with $V_{CE(ON)}$=1.75V.

IGBT for inverter b is IRGP50B60PD1 with $V_{CE\ (ON)}$ = 2V.

LC at inverter output side L = 5 mH C= 10 μF

Carrier frequency = 4.5 kHz

Figure 13 shows the THIPWM for the three-phase inverter. And the line voltage before filter is shown in Figure 14. Figure 15shows the frequency spectrum of the line voltage which shows the fundamental frequency components and the carrier frequency components. The connection of two parallel inverters with different IGBTs ratings and without the resistor connection produces unbalance currents at the output of each inverter side as shown in Figure 16. Figure 17 shows the balance currents after resistor connection. Figure 18 shows the phase voltage and phase current on the load side. The THD for the voltage and current are shown in Figure 19 and Figure 20 respectively

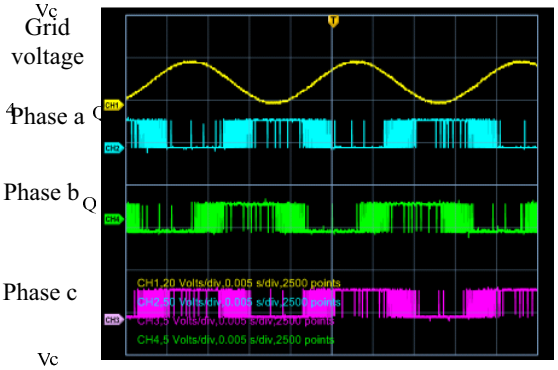


Figure 13: three-phase THIPWM Synchronized with the Grid Voltage (5V/div, 5ms/div)

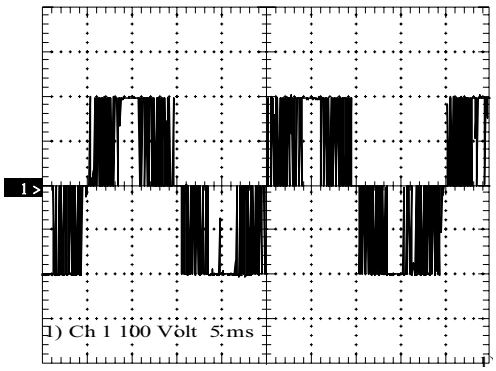


Figure 14: The line voltage before connecting the filter (100V/div, 5ms/div)

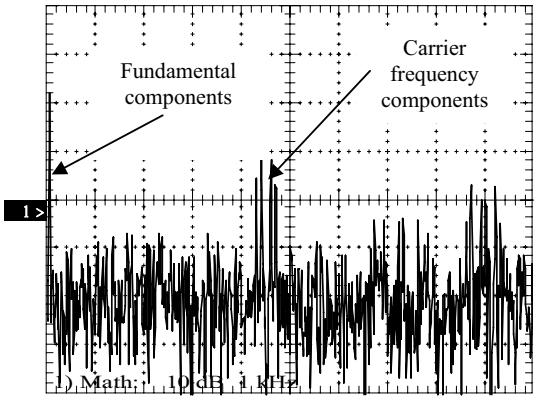


Figure 15: Frequency spectrum of the line voltage (10dB/div, 1kHz/div)

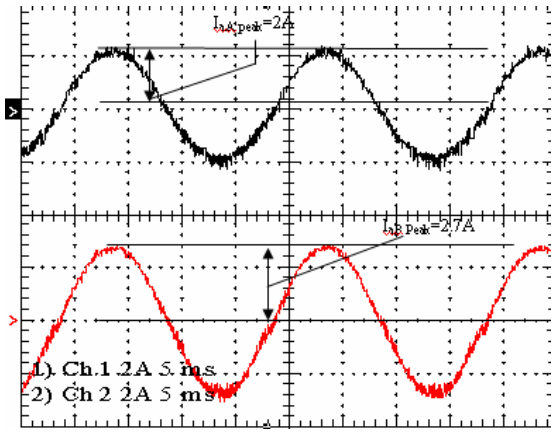


Figure16: Current at each inverter output without resistor connection. (2a/div, 5ms/div)

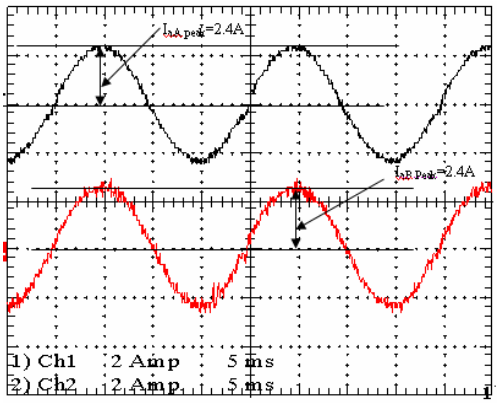


Figure 17: Current at each inverter output with resistor connection. (2a/div, 5ms/div)

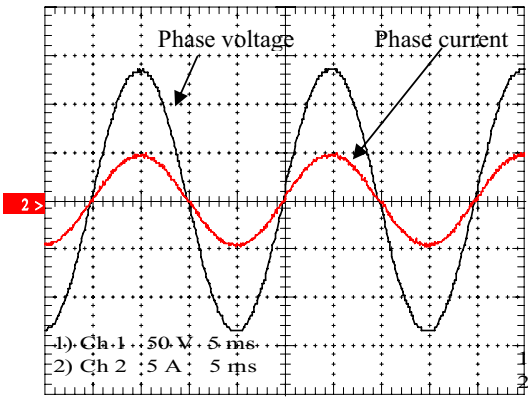


Figure 18: Phase voltage and phase current on the load side (50V/div, 5A/div, 5ms/div)

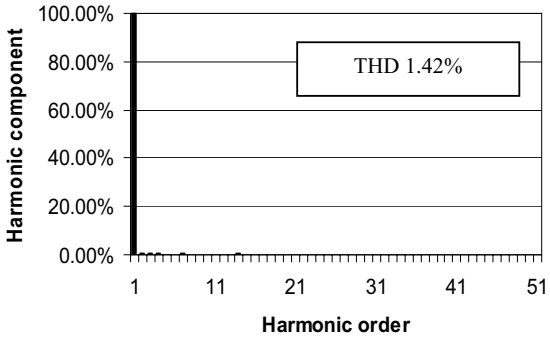


Figure 19: Harmonic spectrum of the phase voltage

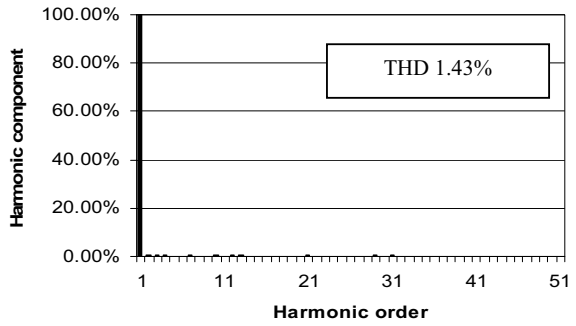


Figure 20: Harmonic spectrum of the phase current

With the connection of two inverters in parallel the total harmonic distortion (THD) on the output voltage and current is less than single inverter. Table 2 shows the harmonic distortion in each case using the phase voltage and phase current.

Table 2: Comparison between Parallel Inverters and Single Inverter in Input and Output Power, Current THD and Voltage THD.

| Inverter | Input power (W) | Output power (W) | η | Current THD | Voltage THD |
|---|---|---|---|---|---|
| Single | 930 | 909 | 97.7% | 1.42% | 1.43% |
| Double | 945 | 930 | 98.4% | 1.36% | 1.28% |

## VII. CONCLUSION

This paper presents a Parallel connected three-phase inverter. The improvement of parallel connection over single inverter is clearly shown. By comparing the THD and efficiency in single unit and parallel connected unit the THD improve and the efficiency as well. The THD reduced to be less than 1.5% for the current and the voltage. The power capability of the inverter system will be higher by connecting the inverters in parallel. The two inverters are sharing the same current value which reduces the circulating current to minimum.

## REFERENCES

[1] I. J. Pitel, S. N. Talukdar, and P. Wood, "Characterization of Programmed-Waveform Pulse-Width Modulation," IEEE Transactions on Industry Applications, Vol. IA-16, Sept./Oct. 1980, pp. 707–715.

[2] Fainan A. Magueed, and Jan Svensson, "Control of VSC connected to the grid through LCL filter to achieve balanced currents," in Proc. IEEE Industry Applications Society Annual Meeting 2005, vol. 2, pp. 572-578

[3] N. Mohan, "A Novel Approach to Minimize Line- Current Harmonics in Interfacing Power Electronics Equipment with 3-Phase Utility Systems", IEEE Trans on Power Delivery, Vol. 8, p1395-1401. July, 1993

[4] Naik. N, Mohan, N. ; Rogers, M. ; Bulawka, "A novel grid interface, optimized for utility-scale applications of photovoltaic, wind-electric, and fuel-cell systems", IEEE Trans on Power Delivery, vol.10, Oct. 1995, pp. 1920-6

[5] Lohner, A.; Meyer, T.; Nagel, A. A new panel-integratable inverter concept for grid-connected photovoltaic systems. ISIE '96. Proceedings of IEEE International Symposium on Industrial Electronics, Warsaw, Poland, 17-20 June 1996, pp. 827-31 vol.2.

[6] Hatziadoniu, C.J.; Chalkiadakis, F.E.; Feiste, V.K. A power conditioner for a grid-connected photovoltaic generator based on the 3-level inverter. IEEE Transactions on Energy Conversion, vol.14, (no.4), IEEE, Dec. 1999, pp. 1605-10.

[7] F. Blaabjerg, Z. Chen, S. B. Kjaer "Power Electronics as Efficient Interface in Dispersed Power Generation Systems", IEEE Transactions on Power Electronics, vol. 19, No 5, 2004.

[8] SIMULINK help

**Mr. Mahmoud A. A. Younis** was born in Gaza, Palestine. He receives the B.Sc. degree from IIT, Bangladesh in 1997, and the M.Sc. degree from UM Malaysia. in 2001. Currently he is a lecturer in the Department of Electrical Engineering, university industry selangor (UNISEL) , Malaysia, and he is doing PHD in the Department of Electrical Engineering, UM, Malaysia . Mr. Mahmoud is active in Power Electronics research Group in UM and His research interest including, Power Electronics, Industrial Electronics and Fuel cell system

**Prof. Dr. Nasrudin Abd Rahim** received the B.Sc(Hons) in Electrical and Electronics Engineering and M.Sc (Electrical Power Engineering) degrees from University of Strathclyde, U.K in 1985 and 1988 respectively. He received the Ph.D from Heriot-Watt University, U.K in 1995. He is currently a Professor in the Department of Electrical Engineering, University of Malaya and headed the Center for Research Power Electronics & Drives, Automation and Control. He has conducted research and advanced development of power converters for the three-phase flyback voltage isolation, ac and dc motor drives, active power filter design, utility interactive photovoltaics, battery charger and energy efficiency application. He is the author of more than 100 publications concerning power electronics and motor drives. He is a qualified Chartered Engineer and a cooperate member of The Institutions of Electrical Engineers (U.K). He is also a member of the Institute of Electrical and Electronics Engineers IEEE. He is research interests include power conversion techniques, high power PWM converters, modeling and control of power converters, energy efficiency and electrical drives control.

**Associated Prof. Dr. Saad Mekhilef** received the B. Eng. degree in Electrical Engineering from University of Setif in 1994, and Master of Engineering science and PhD from University of Malaya 1998 and 2003 respectively. He is currently a lecturer at Department of Electrical Engineering; University of Malaya. Dr. Saad is the author and co-author of more than 60 publications in international journal and proceedings. He is actively involved in industrial consultancy, for major corporations in the power electronics projects. His research interests include industrial electronics, power conversion techniques, control of power converters, renewable energy and energy efficiency