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A Novel Low Power Digitally Controlled Oscillator with Improved linear Operating Range

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***Abstract*—**In this paper, an ultra low power and low jitter 12bit CMOS digitally controlled oscillator (DCO) design is presented. Based on a ring oscillator implemented with low power Schmitt trigger based inverters. Simulation of the proposed DCO using 32nm CMOS Predictive Transistor Model (PTM) achieves controllable frequency range of 550MHz~830MHz with a wide linearity and high resolution. Monte Carlo simulation demonstrates that the time-period jitter due to random power supply fluctuation is under 31ps and the power consumption is 0.5677mW at 750MHz with 1.2V power supply and 0.53-ps resolution. The proposed DCO has a good robustness to voltage and temperature variations and better linearity comparing to the conventional design.

***Keywords*—**digitally controlled oscillator (DCO), low power, jitter; good linearity, robust

I. Introduction

PHASE-LOCKED loops (PLLs) are widely used in many communication systems to clock and data recovery or frequency synthesis [1]. Typical analog PLLs include a phase-frequency detector, a charge pump, a loop filter, a voltage controlled or current controlled oscillator, and a frequency divider [2], [3]. The controlled oscillator is the key component in the core of PLL. Recently, efforts have been made toward the development of fully digital PLLs. Compared to their analog counterparts, fully digital PLLs exhibit better noise immunity and they are invulnerable to DC offset and drift phenomena [4], [5], [6]. Digitally controlled oscillator (DCO) is a replacement of the conventional voltage or current controlled oscillator in the fully digital PLLs. DCO is the heart of the ADPLL that shows higher noise immunity and robustness than the conventional PLLs [1]. DCO dominates the major performances of ADPLL such as power consumption and jitter, and hence is the most important component of such clocking circuits [4], [6], [7]. Since DCO occupies 50% power consumption of an ADPLL [7], the power consumption of DCO should be reduced further to save overall power dissipation to meet low power demands in SOC designs.The Block diagram of the ring oscillator based DCO which is used in this paper is shown in Fig 1. It consists of digitally controlled delay elements which are controlled by coarse and fine bits and a control logic block for enabling DCO and linearization circuit for linearizing the DCO period by increasing the input code. DCO starts to work by applying the initial value to the circuit.Basically, two main techniques exist for designing the DCO as shown in fig. 2. One technique changes the MOS driving strength dynamically using a fixed capacitance loading and achieves a fine resolution [8], [9]. While the other uses shunt capacitor technique to tune the capacitance loading [10], [11]. They both have good linear frequency response and a reasonable frequency operating range. Power consumption is an important problem for portable battery charged computing systems, so the reduction of the power consumption has become a major concern.A simple DCO that directly uses an inverter ring is presented in [12], but has insufficient resolution for most appli

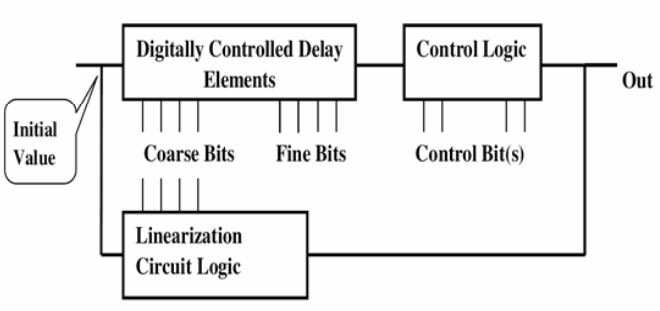

Fig. 1 Block diagram of the ring oscillator DCO

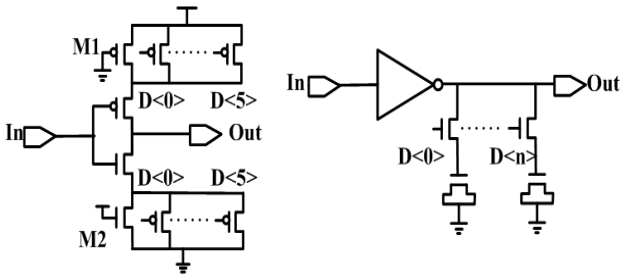

Fig. 2 Standard Cell of Digitally controlled oscillator. (a) Driving strength controlled. (b) Shunt capacitance controlled.

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applications. Another DCO example consists of bank of tri-state inverter buffers [13]. The delay resolution in this case can be controlled by the number of enable buffers. However, [13] has the disadvantages of large silicon area and high power consumption. Another means of fine resolution enhancement, implemented by an Or-And-Inverter (OAI) cell shunted with two tri-state inverters to enhance driving capability, was proposed in [3]. The proposed DCO in [3] has less area and power consumption than [13]. However, the resolution step of the proposed DCO is nonuniform and sensitive to power-supply variation because it uses OAI cell to change the delay resolution, this technique also requires an additional decoder for mapping OAI cell control input.This paper presents a low power, low jitter and high resolution DCO using binary controlled pass transistors and low power Schmitt trigger. The DCO is designed using the 32nm CMOS Predictive Transistor Model (PTM) and HSPICE simulator.

II. Conventional and proposed DCO architecture

DCO should generate an oscillation period of T_{DCO}, which is a function of digital input word D and given by:

$$T_{DCO} = f(d_{n-1}2^{n-1} + d_{n-2}2^{n-2} + ... + d_1 2^1 + d_0 2^0) \quad (1)$$

the DCO transfer function is defined such that the period of oscillation T_{DCO} is linearly proportional to digital word D with an offset

$$T_{DCO} = T_{offset} - D.T_{step} \quad \text{D:Digital control bits} \quad (2)$$

where T_{offset} is a constant offset period and T_{step} is the period of quantization step. For the conventional driving strength controlled DCO shown in Fig. 3, the delay tuning range of this standard cell is obtained as follows:

$$\frac{T_{une}}{2} = (C_1 - C_2)(R_1 \| \frac{\Delta R}{d_0} \| \frac{\Delta R}{d_1 2} \| ... \| \frac{\Delta R}{d_{n-1}2^{n-1}}) - (C_1 + C_2)R_1 \quad (3)$$

$$= \frac{R_1(C_1 + C_2)}{1 + (D.\Delta W)/W_1} - (C_1 - C_2)R_1 \quad (4)$$

$$\approx R_1(C_1 + C_2)\frac{D.\Delta W}{W_1}, \quad (\text{Only if } \frac{D.\Delta W}{W_1} \ll 1) \quad (5)$$

where R_1 is the equivalent resistance of M1 and W1 is the width of M1. In order to have a good linear tuning range, the width of transistor M1 has to be increased as can be seen in Equation (5). Consequently, the equivalent resistance R_1 will decrease resulting in a smaller delay tuning range. One way to increase the tuning range while keeping the linear response is to increase the capacitance loading. However this will minimize the maximum frequency that the DCO can accomplish and the power consumption will also be increased.

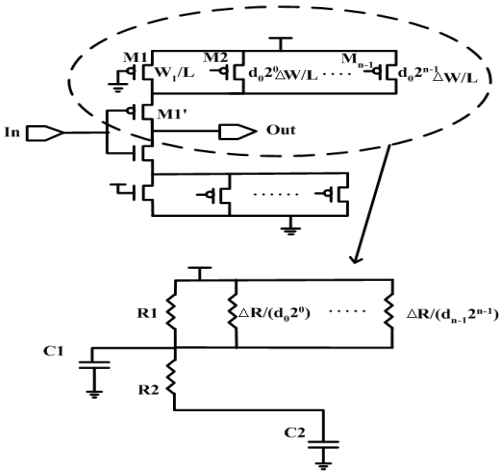


Fig. 3 Equivalent circuit for the calculation of delay tuning range

The proposed DCO is based on ring oscillator implemented with low power Schmitt trigger based inverters. It uses binary controlled pass transistor arrays to control the period of DCO. Schmitt trigger based inverter has a higher low to high switching threshold and lower high to low switching threshold compared to the conventional As a result, the proposed DCO circuit provides the same tuning range with smaller capacitance loading, which is beneficial for power consumption reduction [15]. Moreover, in conventional DCO circuit, the slope of the input signal to each stage decreases gradually due to the large delay between each stage. This result in not only non-ideal rail-to-rail switch but also a poor power performance. The steep slope of the output signal from the Schmitt trigger based inverter minimizes this problem to certain extend. The improved DCO has two coarse delay cells and two fine delay cells and a NAND gate for reset. We don't use the Schmitt trigger in fine delay cells of DCO, because Schmitt trigger transistors are switched in each cycle, so they themselves consume a lot of power in the DCO therefore omission of Schmitt trigger from fine delay cells can decrease the power consumption of the circuit. Since fine delay cells of DCO do not have a capacitance loading thus fine delay cells output signal is still sharp and omission of the Schmitt trigger from fine delay cells does not disturb the DCO performance. Furthermore we use the low power Schmitt trigger in coarse delay cells which has two inverters in its structure and these inverters act as buffers in the signal path and by reconstructing the signal, reduce the jitter of the DCO. This Schmitt trigger is reported in [14]. The high to low and low to high switching threshold of the Schmitt trigger is obtained as follows

$$V_{TR} = \frac{V_{tn} + \sqrt{K_n/K_p}(VDD - V_{tp})}{1 + \sqrt{(\frac{K_n}{K_p})}} \quad (6)$$

Where Kn and Kp are the transconductance factors of Mn_{inv} and $Mp_{inv,}$ and Vtn and Vtp are their respective threshold voltages. The circuit diagrams of the conventional DCO and proposed DCO are showed in Fig. 4. In order to compare the power consumption, both circuits must be equally sized.

III. Comparison of Power Consumption between the Conventional and Proposed DCO Structures

Two structures of DCO are simulated and compared using 32nm CMOS PTM (Predictive Transistor Model) with a supply voltage of 1.2Volts and HSPICE simulator. The impact of each control bit on the period of the two DCO structures is shown in table 1. Both structures have the same linear tuning range until 5th bit is asserted. This is due to the fact that the requirement for linear tuning range fails when D.ΔW becomes too large comparing to W1 so these structures are linear for the first 32 input coarse codes. In order to compare the power consumption, the first 5 control bits are chosen instead of 6, since the last control bits contributes to non-linear tuning range which is not desired for DCO. Moreover, since two DCO structures have the same operation ranges, it is more reasonable for us to compare their power consumption. Compared to the conventional DCO, the

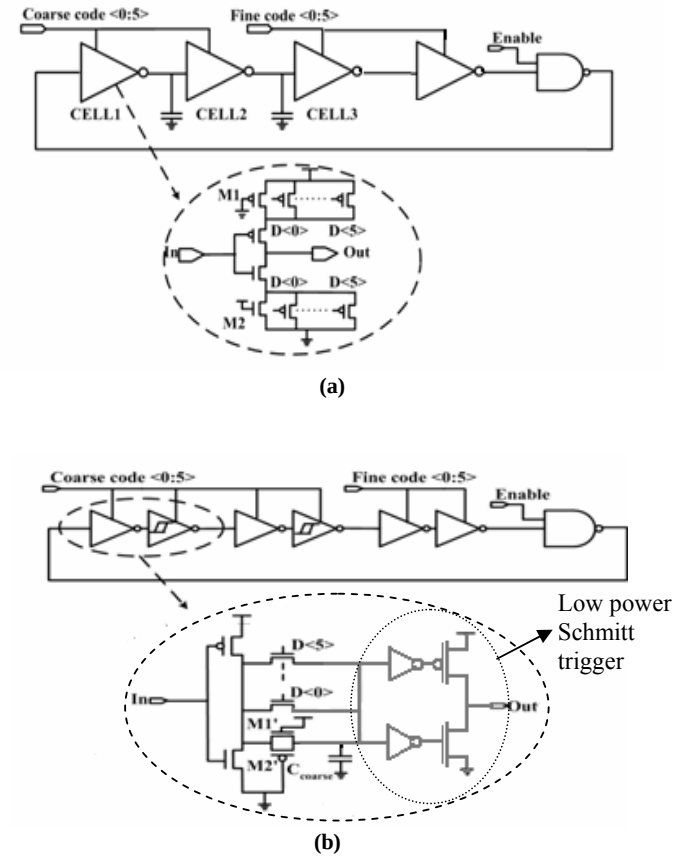


Fig. 4 Digitally Controlled Oscillator. (a) Conventional DCO structure, (b) proposed DCO structure

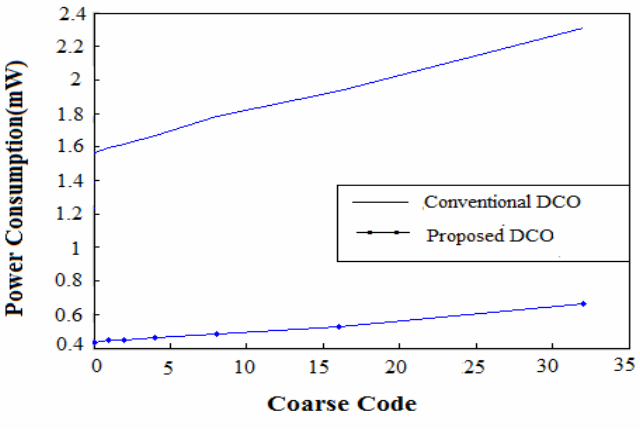


Fig. 5 Power consumption of the two DCO structures

proposed DCO saves approximately 70% power consumption as shown in fig 5. As discussed in section II, this reduction is due to the comparatively smaller capacitance loading for the Schmitt trigger based inverter than the conventional inverter at the same operating frequency and using the low power Schmitt trigger in the inverters of coarse delay cells. The proposed DCO is more power efficient than the conventional DCO.

TABLE I
IMPACT OF EACH CONTROL BIT ON THE DCO PERIOD

Control bits	Conventional DCO		Proposed DCO	
	Period (ns)	Delta (ps)	Period (ns)	Delta (ps)
100000	1.1905	246.7	1.1902	242.8
010000	1.4372	124.5	1.4330	134.8
001000	1.5617	84.5	1.5678	91.6
000100	1.6462	42	1.6594	32.7
000010	1.6882	20.1	1.6921	18.1
000001	1.7083	21.9	1.7102	19.9
000000	1.7302	-	1.7301	-

IV. Improving Linear Operating Range of the Proposed DCO and Simulation Results

The proposed DCO which is explained in section II has a limited linear operating range as discussed above. In this paper, three stage constant delay chains and 4:1 multiplexer are used to increase the operating range [15], the proposed DCO and its linearization circuit are shown in Fig. 6. The 6th bit is taken off for better linear response and the 1st bit is also taken off for larger coarse resolution. So this structure is linear for 64 input coarse codes instead of 32 input coarse codes. The proposed DCO structure with increased operating range is designed and simulated using 32nm CMOS PTM model and HSPICE simulator. The frequency ranges of the coarse and fine tuning loops are shown in Fig. 7. The curves have a good linearity which is a key factor of the PLL performance. The operational frequency response to the process, temperature and voltage variations are shown in Fig. 8. The curves show the normalized data with respect to

the center frequency. Fig. 8 shows that the relative delay per code is almost the same regardless of the process, temperature and voltage variations, which means this DCO design is robust to PVT variations. We can extend the linearization circuit to achieve a 14-bit DCO which is linear for 128 input coarse codes. Extended linearization circuit is shown in Fig. 9. It consists of a seven stage constant delay chain and 8:1 Mux. The 7^{th} and 6^{th} bits are taken off for better linear response and 1^{st} bit is also taken off for better coarse resolution. The simulation results show that the DCO curve has a good linearity. The frequency ranges of the coarse tuning loop are shown in Fig. 10.

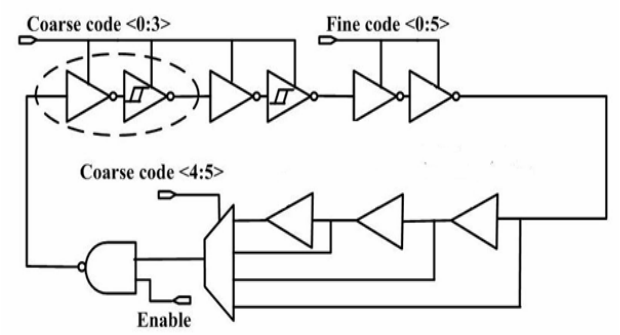
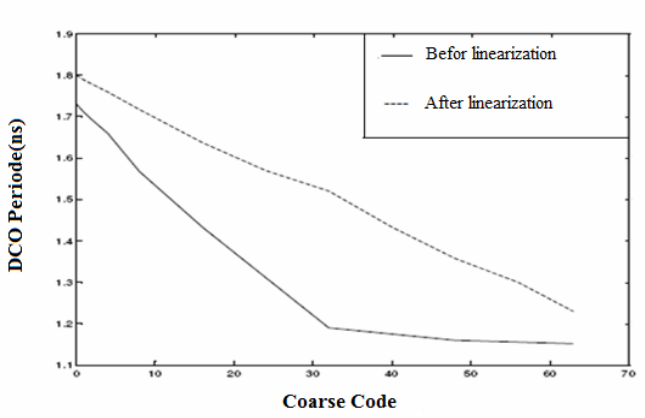
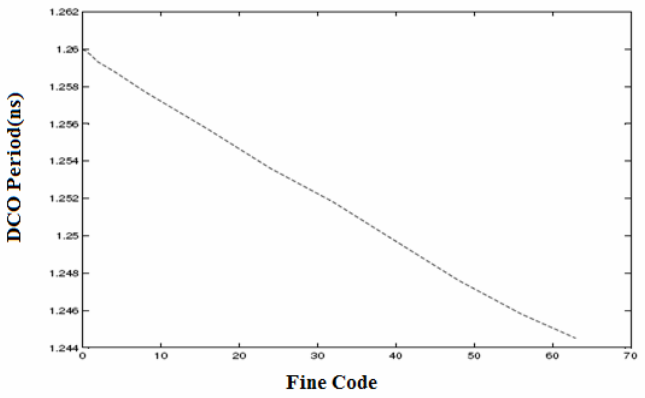


Fig. 6 The proposed DCO structure with improved linear operating range

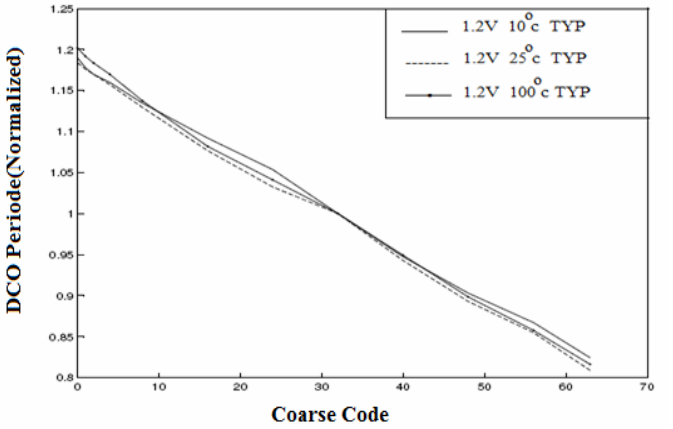


(a)



(b)

Fig. 7 Operating range of the proposed DCO. (a) Coarse loop (b) Fine loop



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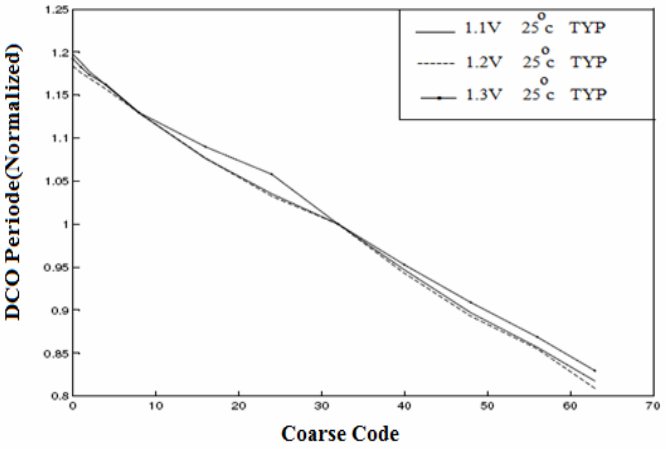
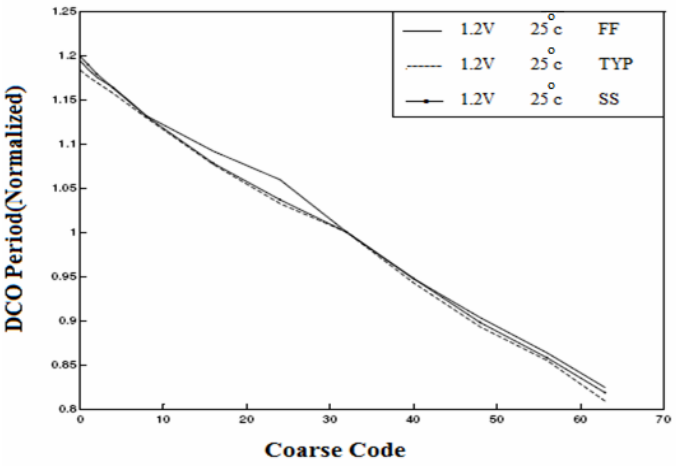


(b)



(c)

Fig. 8 Delay characteristics of the coarse loop according to Process, Voltage and Temperature variations. (a) Temperature Variation, (b) Voltage Variation, (c) Process Variation

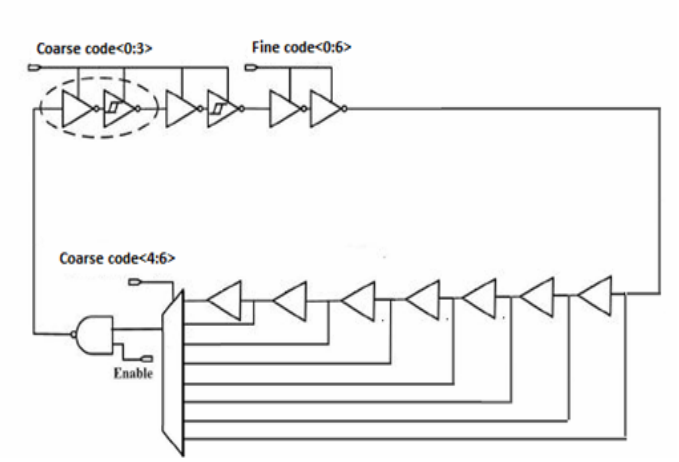


Fig. 9 14-bit proposed DCO structure

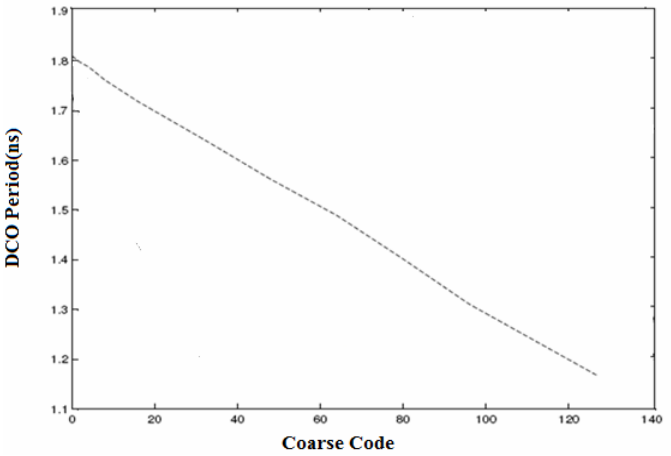


Fig. 10 14-bit DCO structure operating range

The time-period jitter is the time difference between the measured cycle period and the ideal cycle period. The jitter performance of the proposed DCO is simulated by Monte Carlo analysis using a Gaussian distribution function taking into account 10% variation in supply voltage. The results are shown in Fig. 11 by overlapping every cycle period. A 31ps time-period Jitter is measured.

Table 3 shows the measurement results to compare with a few recent state-of-the-arts DCO designs [1], [4], [10], [13].

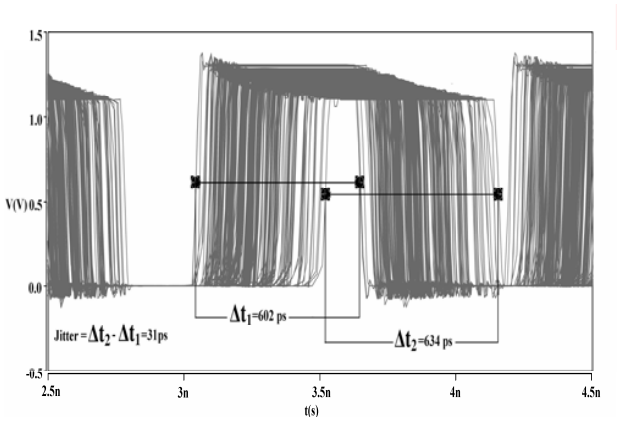


Fig. 11 Time-period jitter of the proposed DCO (Monte Carlo analysis)

TABLE II
CHARACTERISTIC OF THE PROPOSED DCO

Items	Coarse delay	Fine delay
Resolution	6 bit	6bit
Max. DCO Gain	13ps	0.53ps
Avg. DCO Gain	9ps	0.25ps
Operation range	550~830 MHz	
Power consumption	0.5677mW @ 750 MHz	

The proposed DCO achieves the finest LSB resolution and the highest operating frequency. In addition, the proposed DCO consumes less power than the others.

V. CONCLUSION

A low power 12 bit digitally controlled CMOS oscillator (DCO) design for low power consumption and low jitter is presented. The presented DCO demonstrate a good robustness to process, voltage and temperature variations and better linearity comparing to the conventional design. Simulation of the proposed DCOs using 32 nm CMOS Predictive Transistor Model and HSPICE simulator achieves a frequency of 550~830 MHz and power consumption of 0.5677mW at 750 MHz and 1.2V power supply. The performance, flexibility, and robustness make the proposed DCO viable for high performance fully digital PLL application.

TABLE III
COMPARISON WITH EXISTING DCOS.

Function	[13]	[1]	[4]	[10]	Proposed DCO
Process	0.6 um @ 5V	0.35um @ 3.3V	0.35 um @ 3.3V	0.13 um @ 1.65V	32nm@ 1.2V
DCO control word length	10 bits	15 bits	12 bits	8bits	12 bits
Coarse Resolution	550 ps	385 ps	300 ps	-	12 ps
LSB(Fine) Resolution	10 ps	1.55 ps	5ps	40 ps	0.53 ps
DCO output frequency	10 ~12.5 (MHz)	18 ~214 (MHz)	45~450 (MHz)	150(MHz)	550 ~830 (MHz)
Power consumption	164mW@ 100MHz	18mW@ 200MHz	100 mW @ 450 MHz	1mW @ 150MHz	0.5677mW@ 750MHz

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