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High-Resolution 12-Bit Segmented Capacitor DAC in Successive Approximation ADC

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***Abstract*—**This paper study the segmented split capacitor Digital-to-Analog Converter (DAC) implemented in a differential-type 12-bit Successive Approximation Analog-to-Digital Converter (SA-ADC). The series capacitance split array method employed as it reduced the total area of the capacitors required for high resolution DACs. A 12-bit regular binary array structure requires 2049 unit capacitors (Cs) while the split array needs 127 unit Cs. These results in the reduction of the total capacitance and power consumption of the series split array architectures as to regular binary-weighted structures. The paper will show the 12-bit DAC series split capacitor with 4-bit thermometer coded DAC architectures as well as the simulation and measured results.

***Keywords*—**Successive Approximation Register Analog-to-Digital Converter, SAR ADC, Low voltage ADC.

I. Introduction

SUCCESSIVE Approximation Analog-to-Digital Converter (SA-ADC) with charge redistribution based architectures has the advantage of low power operation [1]-[4]. However, as the number of bit increases, input load capacitance and area of binary-weighted capacitor DAC (Digital-to-Analog Converter) too increase exponentially [5]. Fig. 1(a) shows a 12-bit binary weighted capacitor DAC example. Fig. 1(b) and Fig. 1(c) are two split capacitor DAC solutions to reduce both input capacitance and area for binary weighted DAC.

In Fig. 1(b), fractional value bridge capacitor is implemented, so that the two capacitor arrays have the same scaling. In the charge redistribution, the total weight of the left array is equal to the total weight of the lowest bit in the right array. However fractional value for the bridge capacitor causes poor matching with other capacitors. In Fig. 1(c), a unit bridge capacitor is implemented and the dummy capacitor C*dummy* is removed. Thus, the total weight of the left array achieves the same weight as the lowest bit in the right array. However, 1LSB gain error is caused. Both the above implementations are vulnerable to parasitic capacitance in Node A and between Node A and Node B, which causes mismatch between the left and right arrays.

Fig. 1(d) proposes a unit bridge capacitor with 4-bit thermometer coded DAC scheme to improve the linearity performance. As shown in Fig. 1(d), 4 MSB bits on the capacitor array were implemented using the thermometer coded scheme. The proposed DAC are implemented fully differential. Single-ended circuit is shown for simplicity.

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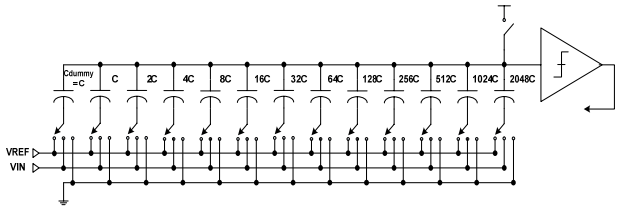

Fig. 1(a) A conventional 12-bit binary weighted capacitor DAC

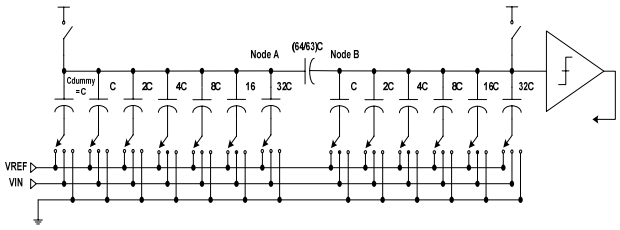

Fig. 1(b) 12-bit DAC with fractional value bridge capacitor

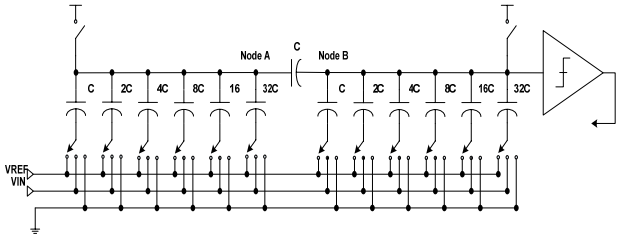

Fig. 1(c) 12-bit DAC with unit value bridge capacitor

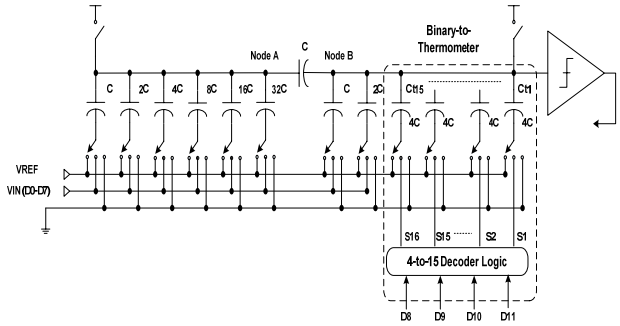

Fig. 1(d) 12-bit with 4-bit thermometer coded DAC

II. Overall SARADC Operation

The architecture of a SAR ADC is shown in Fig. 2, consisting of a series structure of a capacitive DAC, a comparator and successive approximation (SA) control logic [6]. The SA control logic includes shift registers and switch drivers which control the DAC operation by performing the binary-scaled feedback during the successive approximation. The DAC capacitor array is the basic structure of the SAR ADC and it serves both to sample the input signal and as a DAC for creating and subtracting the reference voltage.

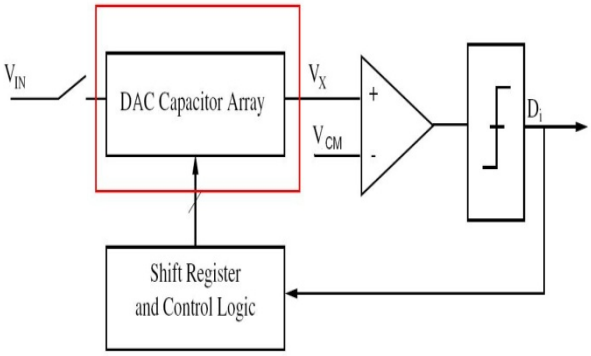

Fig. 2 Architecture of a SAR ADC

III. Implementation

A. Capacitor Structure Design

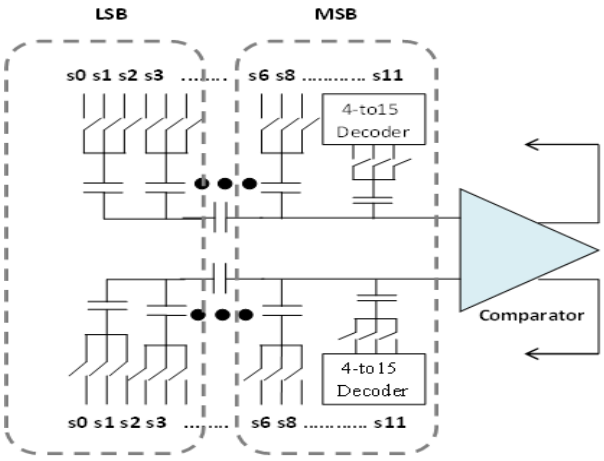

Fig. 3(a) A fully differential DAC

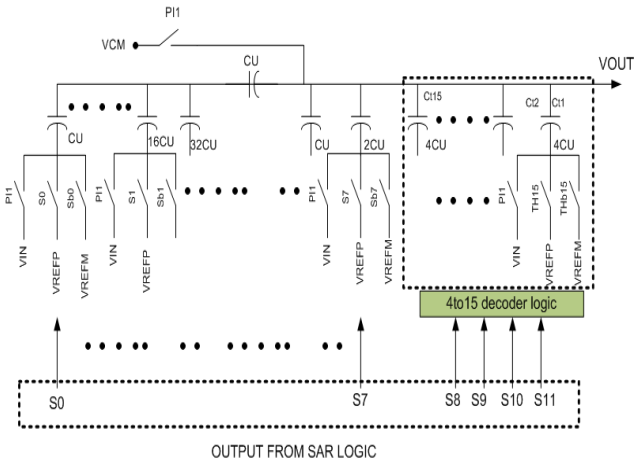

Fig. 3(b) Single-ended DAC

The fully differential DAC consists of two arrays of unit bridge capacitor banks, a fully differential buffer and a4-to-15 decoder where thermometer code are employed as shown in Fig. 3(a). Single-ended circuit is shown for simplicity in Fig. 3(b). The 12-bit DAC was designed with split unit bridge capacitor to help reduce the size of the capacitors required, eventually minimizes the current required to charge up the capacitor array. Combination of sub-DAC and thermometer coding employed to improve linearity especially when major bit transition concerned.

B. Comparator

The comparator circuit comprises of pre-amplifier and latch, shown in Fig. 4(a) . It represents an important part of the SAR ADC since it has to be accurate to the value of the Least Significant Bit (LSB) of an N-bit DAC. For a 12-bit ADC with the reference voltages of +/-1V, the LSB value is approximately 488uV. Therefore, the comparator designed has to resolve a minimum of 488uV difference between the inputs. However, to design such a high performance comparator would require more resources that lead to higher current and power consumption. In this design, a single stage pre-amplifier was used to boost the input voltage before the comparator input. This method relaxes the performance required from the comparator and hence, reduces the current consumed. The comparator used in this design has a latch with minimum-sized devices.

The latch is a regenerative latch Fig. 4(b) , with three distinct phases: PHI1, PHI2 and RESET, where PHI1 and PHI2 are non-overlapping clocks with RESET happening just before PHI1. The latch is simulated across Monte Carlo variation and the maximum offset is 150mV as shown in Fig. 4(c). Thus, the previous stage pre-amplifier has a requirement to amplify the smallest resolvable signal to at least 150mV to the latch input.

The required gain is therefore:

Gain required = 150mV/488uV = 307.4 = 49dB

The simulated gain of the pre-amp is 77B, which is well over the gain requirement.

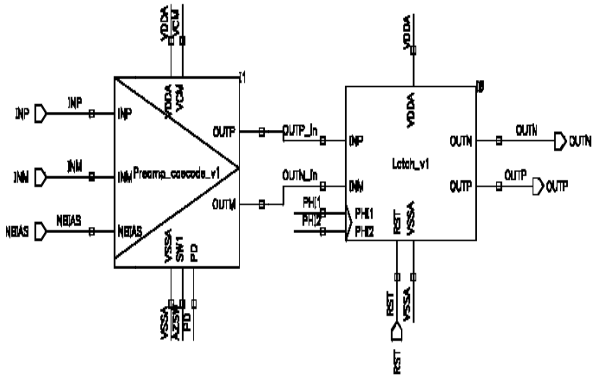

Fig. 4(a) Comparator circuit

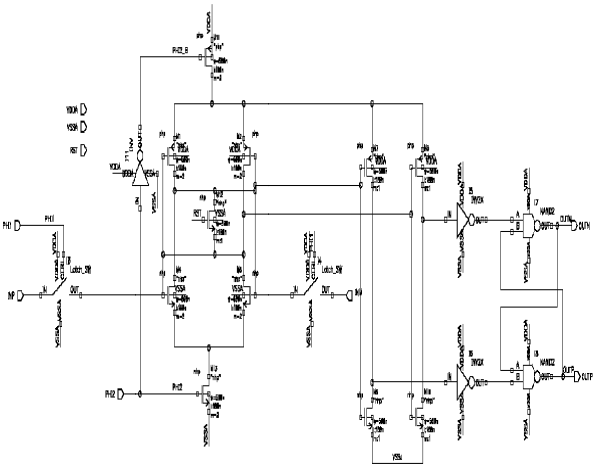

Fig. 4(b) Latch circuit

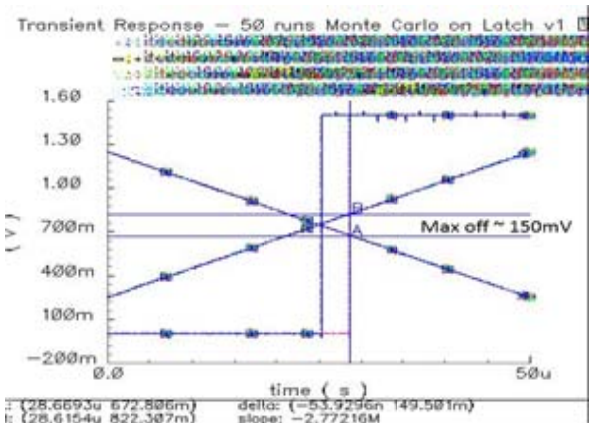

Fig. 4(c) Monte Carlo simulation on Latch circuit

The pre-amplifier is designed to work at down to 1.4V, with a folded-cascode configuration, Fig. 4(d). Folded-cascode architecture was chosen due to the limited headroom available at a minimum VDD of 1.4V for the 0.18um Silterra process. It also provides a better gain performance compared to the conventional single-stage amplifier.

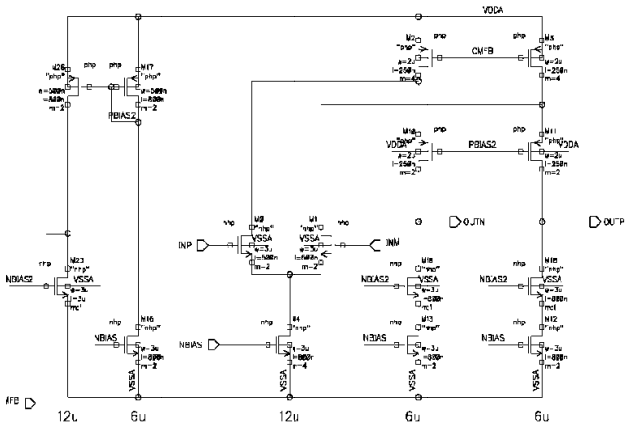

Fig. 4(d) Pre-amplifier circuit

Fig. 5(a) shows the layout implementation of the DAC while Fig. 5(b) shows full implementation of 12-bit SAR ADC.

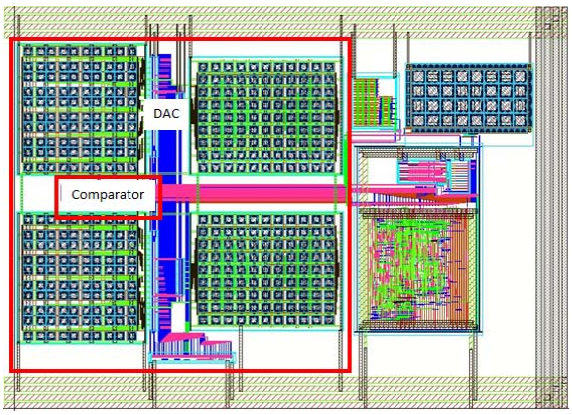

Fig. 5 (a) Layout implementation of the DAC

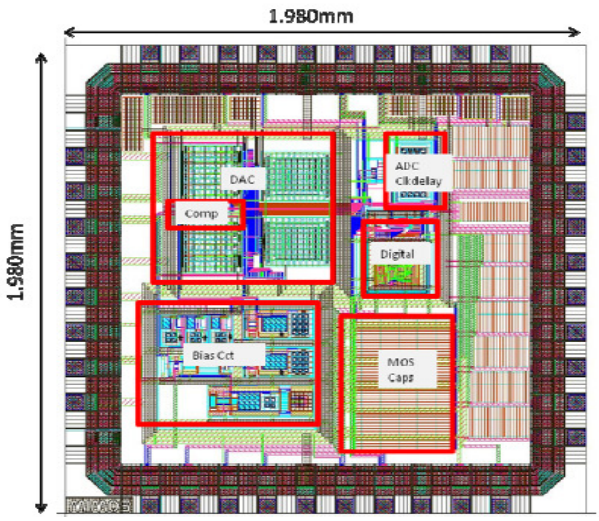

Fig. 5(b) Full layout implementation of the 12-bit SAR ADC

IV. Result

Fig. 6(a) shows schematic simulation and Fig. 6(b) shows post layout simulation during input linearity ramping. Ramping up and ramping down methods is used to test the DAC's linearity. The output for the first ramp up signal shows non-linear at MSB due to the initial common mode value. Subsequent ramp up shows that the output signal is actually linear.

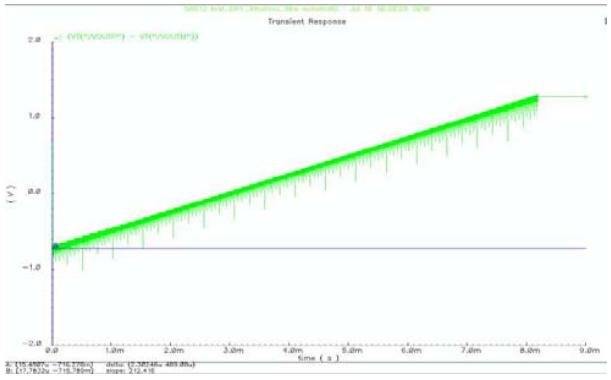

Fig. 6 (a) Schematic simulation

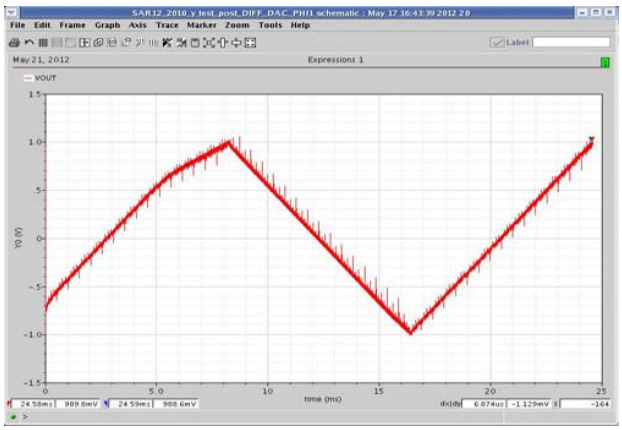

Fig. 6 (b) Post layout simulation

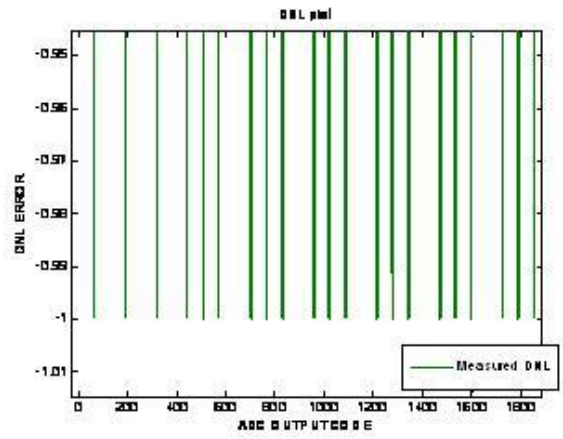

Fig. 7 (a) Measured DNL

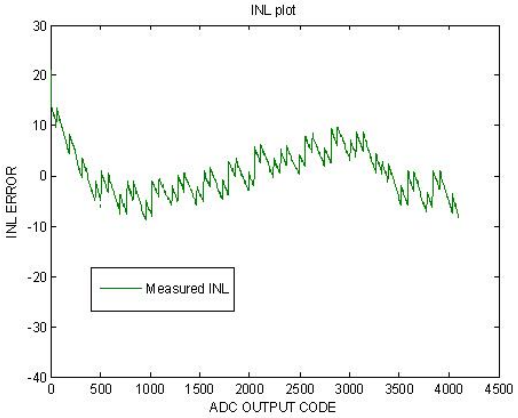

Fig. 7 (b) Measured INL

INL and DNL plot shows that the error is more than ±½ LSB. This may be due to extra parasitic added during layout implementation. This was not captured during post layout simulation since the simulation concentrate more towards major code transition. Fig. 7 (a) and 7(b) are measured DNL and INL plot respectively.

V. Conclusion

A segmented split capacitor Digital-to-Analog Converter (DAC) had been implemented in a differential 12-bit Successive Approximation Analog-to-Digital Converter. Measurement result shows high INL and DNL error due to added parasitic effect during layout. Better layout matching and shielding method should be implemented to further improve the performance.

References

[1] S. Long, J. Wu, X. Xia, L, Shi, A1.8V 3.1mW SuccessiveApproximation ADC in Systemon-Chip, Springer Science +Business Media, LLC 2008.

[2] A. Basu, V. Lee, A. Ma, A 10-bit 10MS/sSuccessive Approximation A/D Converter in0.35um CMOS, University of Michigan, 2002.H. Poor, *An Introduction to Signal Detection and Estimation*. New York: Springer-Verlag, 1985, ch. 4.

[3] D. Draxelmayr, "A 6b 600MHz 10mW ADC Array in Digital 90nm CMOS," ISSCCDig. Tech. Papers, pp. 264-265, Feb. 2004.

[4] N. Verma and A. Chandrakasan, "An Ultra Low Energy 12-bit Rate-Resolution ScalableSAR ADC for Wireless Sensor Nodes," IEEE J. Solid-State Circuits, vol. 42, no. 6, pp.1196--1205, Jun. 2007.

[5] R. J. Baker, H. W. Li, and D. E. Boyce, CMOS Circuit Design, Layout and Simulation.New York: IEEE Press, 1998.

[6] Ji-Yong Um, Digital-domain calibration of split-capacitor DAC with no extra calibration *DAC* for a differential-type SAR ADCSolid State Circuits Conference (A-SSCC), 2011 IEEE Asian.

[7] Ikeda Y, A 14-bit 100-MS/s digitally calibrated binary-weighted current-steering CMOS DAC without calibration ADC, Solid-State Circuits Conference, 2007. ASSCC '07. IEEE Asian.

[8] YanfeiChen, Split capacitor DAC mismatch calibration in successive approximation ADC, Custom Integrated Circuits Conference, 2009. CICC '09. IEEE.