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An Inductive Coupling Based CMOS Wireless Powering Link for Implantable Biomedical Applications

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***Abstract*—**A closed-loop controlled wireless power transmission circuit block for implantable biomedical applications is described in this paper. The circuit consists of one front-end rectifier, power management sub-block including bandgap reference and low drop-out regulators (LDOs) as well as transmission power detection / feedback circuits. Simulation result shows that the front-end rectifier achieves 80% power efficiency with 750-mV single-end peak-to-peak input voltage and 1.28-V output voltage under load current of 4 mA. The power management block can supply 1.8mA average load current under 1V consuming only 12μW power, which is equivalent to 99.3% power efficiency. The wireless power transmission block described in this paper achieves a maximum power efficiency of 80%. The wireless power transmission circuit block is designed and implemented using UMC 65-nm CMOS/RF process. It occupies 1 mm × 1.2 mm silicon area.

***Keywords*—**Implantable biomedical devices; wireless power transfer; LDO; rectifier; closed-loop power control

I. Introduction

WIRELESS power transmission for biomedical applications attracts intensive research interest in recent decades due to the fast development of implantable biomedical systems [1-4] which are currently in tremendous needs for human organ prosthesis [5], daily life health care[6] and clinical treatment [7,8] .

Figure 1 shows the typical system configuration for an implantable biomedical system and its applications. Most of the real time health indicators monitoring systems and bioelectrical prosthesis systems including retinal, cochlear, brain and muscle prosthesis require the device to be implanted underneath the skin, skull or other human body tissues for minimum damage, higher performance and better cosmetic appearance [9-11]. For implanted devices, wireless power and data transmission is preferred to avoid changing battery frequently through surgery. The external power and signal transmission module in Fig.1 transmits the power and data to the implanted devices in the human body through a wireless link. The implanted devices interact with the targeted tissues and cells for biological prosthesis, health monitoring and advanced biomedical treatment such as pain control, mood regulation and remote microsurgery. These bio-information and operation can be monitored and controlled through a handheld device.

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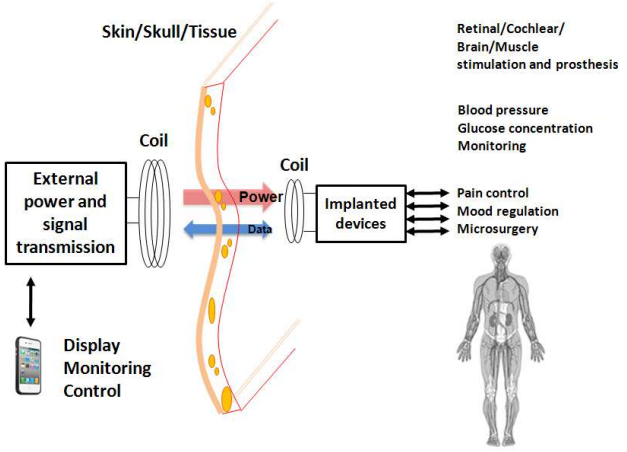

Fig. 1 Block diagram of a typical wireless powering link

There are several concepts and technologies for wireless power transfer since late 19th century [12] including capacitive coupling, inductive coupling, microwave method and laser method. Among these concepts and technologies, inductive coupling is widely used for implantable biomedical systems due to its simplicity and relatively efficient as a short-range near-field wireless power transfer method [13-14]. The typical system architecture of an inductive coupling wireless power transfer system is shown in Fig.2. The dashed line in Fig.2 represents the separation between external power transmission module and the implanted device. The external power transmission module consists of one power amplifier and a primary inductive coil.

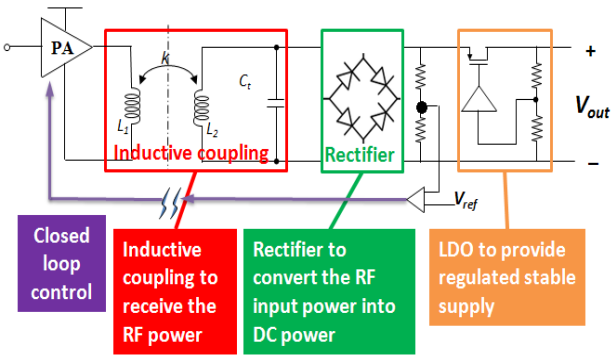

Fig. 2 Block diagram of a typical inductive coupling wireless power link

The power receiving block of the implanted device consists of the secondary inductive coil, matching network, rectifier and low drop-out regulator. The primary and the secondary coils are designed to have a resonant frequency matched to the carrier signal frequency for optimal coupling efficiency. The conventional efficiency-boosting technique adds a capacitor C_t to form the resonance at power carrier frequency. The rectifier is used to convert the differential alternating voltage signal (AC) appearing across the two terminals of secondary coil into a direct voltage signal (DC). To obtain a stable DC supply, one low drop-out voltage regulator (LDO) is followed after the rectifier to provide a regulated DC output to power the entire implanted device.

This paper is arranged as following: Section II describes the detailed circuit design and implementation of wireless power transmission circuit block. Section III shows the simulation results and interfaces to other blocks. Section IV presents the conclusion and discussion.

II. Circuit Design and Implementation

A. Circuit System Architecture

The circuit system architecture described in this paper is shown in Fig. 3. The circuit system consists of one rectifier connected to the power receiving coil, one protective RF limiter to limit the input voltage level, one protective DC limiter to limit the output voltage level, one bandgap reference to provide voltage references, four LDOs to provide stable power supplies for different circuit blocks such as command link (CM) circuits, transmitter (TX), Phase Lock Loop (PLL) and base-band (BB) circuit in the implanted device and one comparator array to provide feedback on the input power level. The input power can be controlled based on the power received by this wireless power receiving circuit.

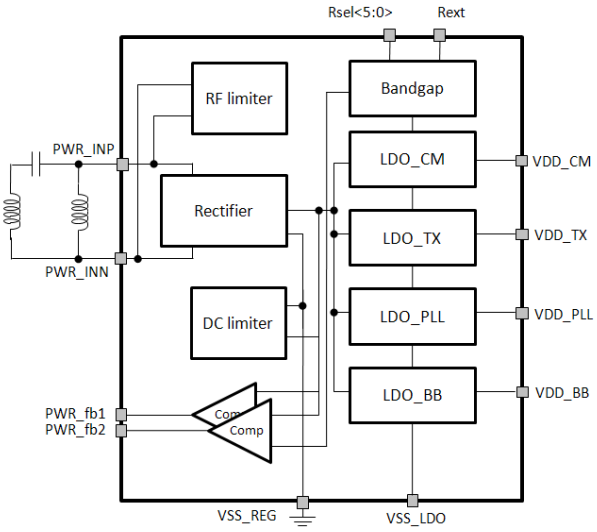

Fig. 3 Circuit system architecture

B. Rectifier, RF and DC limiter

The rectifier circuit design is based on the conventional diode-connected four MOSFETs cross-coupled rectifier design [15]. The required output voltage for rectifier is 1.2 V.

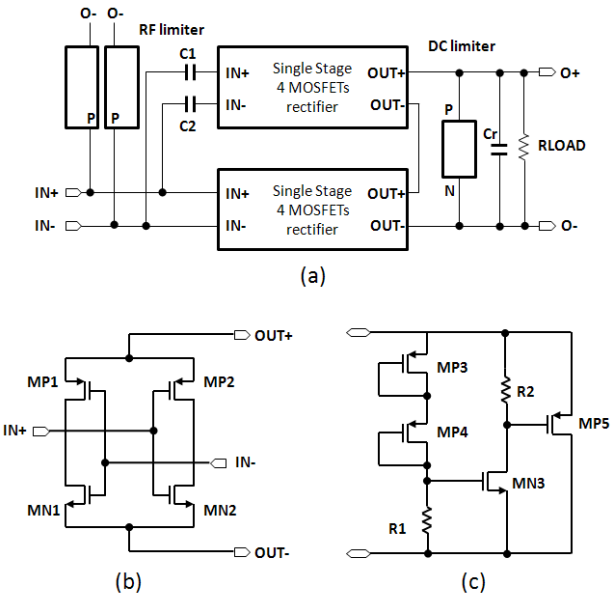

Fig. 4 (a) Top schematic of the rectifier (b) Single stage schematic (c) Schematic of RF/DC limiter

Two-stage architecture shown in Fig.4 (a) is adopted to relax the input voltage requirement for the rectifier. The schematic of the rectifier and RF/DC limiters are shown in Fig.4 (b) and (c), respectively.

Two-stage rectifier architecture is adopted to achieve 1.2-V output DC level under 750-mV single-end peak-to-peak input signal. C1 and C2 are used as coupling capacitors to couple the input signal of the second stage rectifier to the output of the first stage rectifier. The input signal frequency is 1 MHz set by top level system requirement, C1 and C2 is set as 28 nF for effective coupling. Cr is used to reduce the ripple of the rectifier output. The single stage schematic of rectifier is shown in Fig. 4 (b). The negative peak voltage of both input terminals are directed to terminal OUT- and positive peak voltage of both terminals are directed to the terminal OUT+. The load resistance RLOAD is fixed at 250 Ohms in our application. To achieve a high efficiency in the rectifier the MOSFETs in the rectifier is designed to have a very low ON resistance. The size of MP1 and MP2 is 180 ×200 μm / 0.37 μm, the size of MN1 and MN2 is 120 ×32 μm / 0.37 μm. Two RF limiters are connected with input nodes to protect the input of the rectifier from unexpected large voltage signal. One DC limiter is also connected between the rectifier output terminals to protect the circuit blocks following rectifier which are the LDOs in the system. The schematic of the RF / DC limiters are shown in Fig.4 (c). Two diode connected PMOS transistors are used to define the threshold voltage of the limiter. Once the voltage across terminal P and N exceeds the threshold voltage, MN3 will be turned on. The gate voltage of MP5 will approach 0 V causing V_{GS} of MP5 to approach VDD. The input impedance of the limiter becomes very small when the voltage exceeds threshold voltage, compensating the input voltage/power increasing. The threshold voltage for RF limiter is designed as 1 V and threshold voltage for DC limiter is designed as 1.4 V.

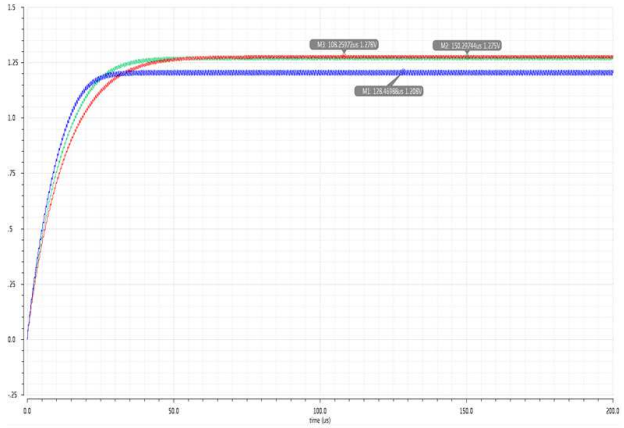

Fig. 5 Simulation results of the two-stage capacitive coupled rectifier

The rectifier is designed and simulated under UMC65nm CMOS / RF process. Cr is chosen as 50nF in the simulation, input voltage source is set as 900 mV single-end peak-to-peak sinusoidal wave with 50 Ohm internal resistance. Fig. 5 shows the simulation results of the rectifier under different process corners. The simulation result shows that the rectifier output is within the design range from 1.2 V to 1.3 V. The simulated power efficiency of the rectifier is 80.2% under the typical process corner.

C. LDO and Bandgap

The power management system of the ASIC consists of one bandgap reference and four LDOs to provide four power domains for the command and data link (CM), phase-locked loop (PLL), baseband digital block (BB) as well as the transmit power amplifier (TX).

In order to operate under 1.2-V supply, the bandgap reference utilizes subthreshold property of MOSFETs to obtain the temperature invariant reference voltage *VREF*. Under subthreshold operation, the gate-source voltage (V_{GS}) of MOSFET exhibits temperature characteristics that are similar to BJTs. As shown in Fig. 6 (a), MN1 and MP5~6 are biased in subthreshold operating region and V_{GS} can be expressed as (1) which is a negative temperature coefficient term [16]

$$V_{GS} = V_{th} + nV_T \ln\left(\frac{I_D}{I_o}\cdot\frac{L}{W}\right) \quad (1)$$

where V_{GS} is the gate-to-source voltage, V_T is the thermal voltage, I_D is the drain current, I_0 is a process dependent characteristic current, L is the effective channel-length, and W is the effective channel-width.

In this design, MP6 has a size that is 8 times larger than MP5. They generate a proportional-to-absolute-temperature (PTAT) current having their gate-source voltage difference across resistor R1. By adding the negative temperature coefficient term V_{GS} with the positive temperature coefficient term, a temperature independent reference voltage *VREF* is generated as expressed in (2)

$$VREF = V_{GS,MN1} + \frac{R2}{R1} nV_T \ln\left(\frac{W_{MP6}}{W_{MP5}}\right) \quad (2)$$

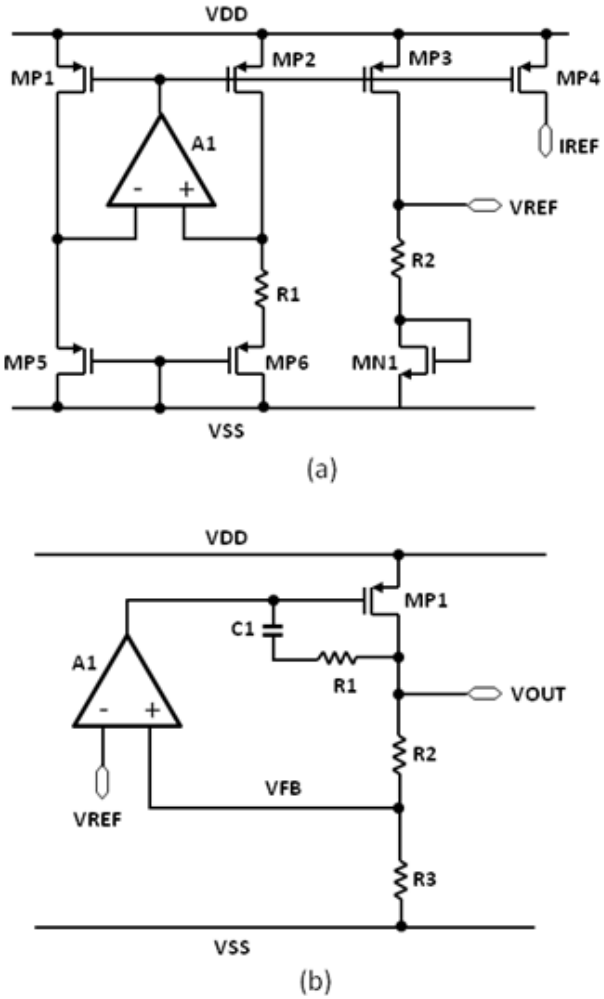

Fig. 6 (a) Schematic of bandgap reference (b) Schematic of LDO

TABLE I
SUMMARY OF POWER MANAGEMENT SIMULATION RESULTS

Parameters	Conditions	Value
VOUT		1.023 V
V_{do}		177 mV
IQ	Bandgap	1.14 µA
	LDO	1.48 µA
I_{out} (max)		10 mA
Line regulation	Low load current	0.8 %/V
	High load current	0.7 %/V
Load regulation		0.004 mV/mA

The VREF is then utilized to generate the supply voltage for the four power domains through LDOs.

The schematic of the LDO is shown in Fig. 6 (b). An amplifier A1 is applied in the feedback mechanism to keep the voltage level at its two input terminals, *VREF* and *VFB* to be equal. The output of A1 adjusts the gate voltage of MP1 to counteract any changes in *VOUT* either due to load current variation or supply variation such that *VFB* keep tracks with *VREF*. Miller capacitor C1 and resistor R1 stabilizes the LDO.

The simulation results of the power management system including bandgap and LDO are summarized in Table I.

III. Simulation Results and Discussions

The wireless power receiver circuit system described in section II is simulated using an ASK modulated RF signal of 1 MHz as the input voltage source. The load is emulated using one 250 Ohm resistor connected to the output of the LDO which is equivalent to 4-mA load current at 1-V supply.

The simulation results are shown in Fig. 7. The rectifier output stables to 1.28 V 2 ms after the initialization. The LDO output is 1.01 V. The 1 MHz CLK is extracted by clock and data recovery (CDR) circuit from the RF input. The two-bit power level <01> from the comparators indicates that the received power is within the optimal power range. POR signal is generated from the POR circuit which is also powered by the LDO. The simulation results demonstrate the functionality of the designed wireless power receiver circuit system with a wireless power transfer capability of 4 mW.

IV. Conclusion

An inductive coupling based CMOS wireless power receiver is designed and implemented using UMC65nm COMS/RF process. The required input RF voltage for the receiver is 750 mV single-end peak-to-peak. The designed output voltage and maximum load current is 1 V and 4 mV respectively to supply other circuit blocks in the implanted device. The entire wireless power receiver achieves 80% power efficiency without considering the inductive coupling loss. This design can be adopted in implantable biomedical applications which require wireless power/data transfer.

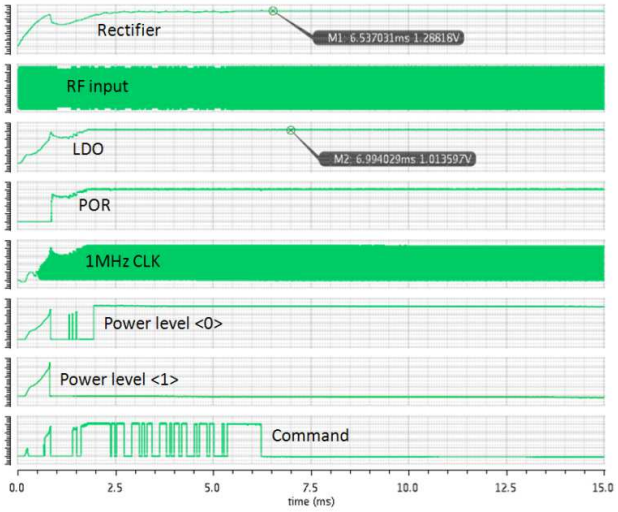

Fig. 7 Simulation results of the close loop wireless power receiver circuit system

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