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Discrete-time Phase and Delay Locked Loops Analyses in Tracking Mode

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***Abstract*—** Phase locked loops (PLL) and delay locked loops (DLL) play an important role in establishing coherent references (phase of carrier and symbol timing) in digital communication systems. Fully digital receiver including digital carrier synchronizer and symbol timing synchronizer fulfils the conditions for universal multi-mode communication receiver with option of symbol rate setting over several digit places and long-term stability of requirement parameters. Afterwards it is necessary to realize PLL and DLL in synchronizer in digital form and to approach to these subsystems as a discrete representation of analog template. Analysis of discrete phase locked loop (DPLL) or discrete delay locked loop (DDLL) and technique to determine their characteristics based on analog (continuous-time) template is performed in this posed paper. There are derived transmission response and error function for 1st order discrete locked loop and resulting equations and graphical representations for 2nd order one. It is shown that the spectrum translation due to sampling takes effect at frequency characteristics computing for specific values of loop parameters.

***Keywords*—**Carrier synchronization, Coherent demodulation, Software defined receiver, Symbol timing.

I. Introduction

PHASE and delay locked loops are the most frequently applied structures in various regulation systems, where the tracked quantity is phase of a signal (or more precisely immediate carrier frequency in communication system) or delay between two signals. Basic motivation for the study of PLL/DLL behavior in discrete domain has been the modernization of universal receiving system for ground station at Department of Radio Electronics. Main requirement of this is to reach high detection efficiency for data signals from experimental satellites with a wide range of bit rates. Therefore the demodulation algorithms have been processed in the digital part of software defined receiver (SDR). This receiver is determined for demodulation of phase shift keying and continuous phase modulations with symbol rates from tens of bauds up to hundreds of kilobauds. Pivotal subsystems of the coherent demodulator are PLL for carrier synchronization and DLL for symbol timing synchronization.

Generally, the PLL or DLL are non-linear systems demanding high-level mathematical computation of high-order non-linear differential equations for determination theirs characteristics, e.g. using Planck-Fokker techniques [1]. Such solution can be simplified by linearization of error detector in tracking mode, where the loop is locked and error value of tracked quantity goes near around equilibrium point. Derivations of analog locked loop characteristics were described in many publications [2], [3], as well as loops in discrete domain based on equivalences with analog forms. Nevertheless, the spectrum translation due to sampling takes effect at resulting frequency characteristics, but in the most of these publications were directly used procedures from analog domain for discrete forms [4]. This phenomenon is the more remarkable the faster response of closed loop is. In following chapters the analyses with sampling implications on resulting frequency characteristics of DPLL/DDLL are executed. The phase or delay loops with fast response bring to bear in the coherent detection of narrow-band satellite signal involved by strong Doppler's effect [5].

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II. Discrete PLL and DLL linearized model

Considering general PLL, results for DLL can be obtained by direct substitution of delay for phase. Block diagram of a linearized PLL in analog domain (APLL) and discrete domain (DPLL) is shown in figure 1. Parameter k_D is the gain of phase error detector in linearized model and it is specified as a ratio between output error value and true error value of input phase. This parameter corresponds to a slope (derivative) of error detector S-curve in equilibrium point. Function $H_{LF}(p)$ is a transmission function of loop filter and k_N is gain of voltage controlled oscillator (VCO). Closed-loop transfer function is defined for phase estimation $\theta_E(t)$ and input phase $\theta(t)$ as a quotient of their transform $\Theta_E(p)$ and $\Theta(p)$. Closed loop transfer function in p-plane for APLL is given by

$$H_{cA}(p)=\frac{\Theta_E(p)}{\Theta(p)}=\frac{k_D k_N H_{LF}(p)}{p+k_D k_N H_{LF}(p)}\ . \quad (1)$$

Closed loop transfer function in z-plane for DPLL can be analogically got by

$$H_{cD}(z)=\frac{\Theta_E(z)}{\Theta(z)}=\frac{k_D k_N H_{LF}(z)}{z-1+k_D k_N H_{LF}(z)}. \quad (2)$$

Another important function describing features of phase locked loops is error function, which defines transmission between error of phase estimation $\Phi(p)$ and input phase $\Theta(p)$. Putting substitution $\Theta_E(p)$ = $\Theta(p)$ - $\Phi(p)$ together with

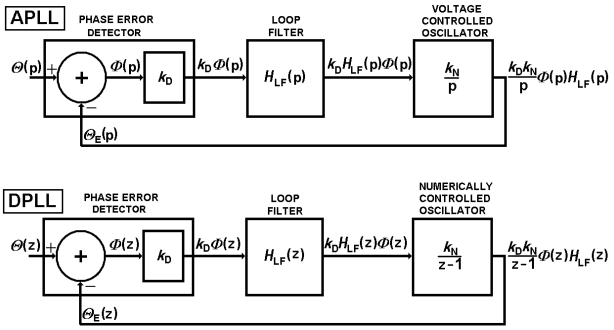

Fig. 1 Linearized model phase locked loop in analog and discrete form

equation (1), the error function in p-plane is

$$H_{eA}(p)=\frac{\Phi(p)}{\Theta(p)}=\frac{p}{p+k_D k_N H_{LF}(p)}=1-H_{cA}(p). \quad (3)$$

The error function in z-plane for discrete form of phase locked loop is

$$H_{eD}(z)=\frac{\Phi(z)}{\Theta(z)}=\frac{z-1}{z-1+k_D k_N H_{LF}(z)}=1-H_{cD}(z). \quad (4)$$

By appropriate choice of the loop filter and its transfer function, any order close loop transfer function and error function can be obtained. In this article only the 1st and 2nd order loops will be taken into consideration. The next chapter derives basic DPLL functions for the simplest configuration of discrete locked loop with 0th order loop filter. The following section is focused on discussion of results for discrete 2nd order loop.

III. Derivation of 1st Order DPLL Characteristics Based on Analog Template

The 1st locked loop contains the 0th order loop filter, it means that the multiplying coefficient k_0 (frequency-independent gain) represents loop filter only. The closed-loop transfer function for continuous implementation is given by equation

$$H_{cA1ord}(p)=\frac{k_D k_N k_0}{p+k_D k_N k_0}=\frac{K_0}{p+K_0}, \quad (5)$$

where $K_0 = k_D \cdot k_N \cdot k_0$. Transfer function defined by formula (5) corresponds to low-pass filter with cut-off frequency $\omega_m = K_0$. Asymptotic slope down of transfer modulus in stop-band is 20 dB/dek. Closed loop transfer function for discrete implementation of 1st order PLL is

$$H_{cD1ord}(z)=\frac{k_D k_N k_0}{z-1+k_D k_N k_0}=\frac{K_0}{z-1+K_0}. \quad (6)$$

The equivalent discrete-time system with continuous-time system, which has low-pass frequency response, can be derived by using impulse-invariance method. This procedure apply the transformation relationship between Laplace transform (p-plane) and Z-transform on poles, it means transform of poles from p-plane to z-plane [3]

$$Z_P = e^{P_P \cdot T_{Sa}}. \quad (7)$$

T_{Sa} is sampling period of discrete system and its value has to satisfy sampling theorem

$$H_{cA}(\omega)=0 \quad for \quad \omega \geq \frac{\omega_{Sa}}{2}, \quad (8)$$

Formulation of single pole of 1st order DPLL, which is derived from APLL system by (7), is

$$Z_P = e^{-\omega_m \cdot T_{Sa}} = e^{-2\pi \frac{\omega_m}{\omega_{Sa}}} = e^{-2\pi \cdot \Omega_m}. \quad (9)$$

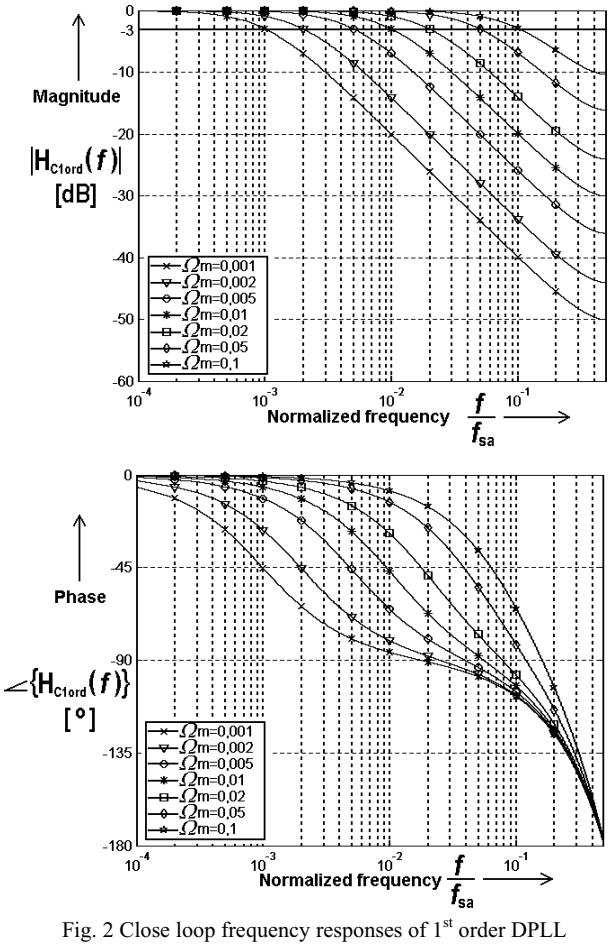

Fig. 2 Close loop frequency responses of 1st order DPLL

Parameter Ω_m is defined as normalized cut-off frequency of 1st order DPLL

$$\Omega_m = \frac{\omega_m}{\omega_{Sa}} = \frac{f_m}{f_{Sa}} \tag{10}$$

and it is possible to set it in range (0, 0.5).

Coefficient K_0 in (6) is derived by confrontation of the pole in (9) and the denominator of closed loop transfer function (6)

$$K_0 = 1 - e^{-2\pi\cdot\Omega_m} \tag{11}$$

Finally, the closed-loop transfer function of 1st order DPLL is given by substitution (11) in (6)

$$H_{cD1ord}(z) = \frac{K_0}{z - 1 + K_0} = \frac{1 - e^{-2\pi\cdot\Omega_m}}{z - e^{-2\pi\cdot\Omega_m}}. \tag{12}$$

Similarly, the error function of 1st order DPLL is determined by formula

$$H_{eD1ord}(z) = 1 - \frac{K_0}{z - 1 + K_0} = \frac{z-1}{z - 1 + K_0} = \frac{z-1}{z - e^{-2\pi\cdot\Omega_m}}. \tag{13}$$

The closed loop frequency response of 1st order DPLL is presented in figure 2, where the slope down of modulus in stop-band less than 20 dB/dec is obvious and this value decreases with growing Ω_m. It is implication of imperfect fulfillment of sampling theorem (8), or effect of aliasing. Because of the aliasing that occurs in the sampling process, the frequency response and behavior of the DPLL is not identical to the original APLL.

The last step of 1st order DPLL analyses is the determination of stability conditions. Single pole of DPLL system is given by formula (9), it lies on real axis inside of unity circle for any Ω_m in possible range (0, 0.5). Due to the 1st order DPLL is unconditionally stable.

IV. 2ND ORDER DPLL CHARACTERISTICS

Analogically as the discrete 1st order locked loop characteristics computation, the 2nd order DPLL characteristics were derived. Block diagram of discrete loop filter for 2nd order PLL is shown in figure 3. There are several configurations of such loop filter, so following calculations represent DPLL system with filter in arrangement in figure 3. The derivation of DPLL characteristics was based on the 2nd order analog PLL with integrator described by closed loop transfer function []

$$H_{cA2ord}(p) = \frac{2\zeta\omega_n p + \omega_n^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}, \tag{14}$$

where ω_n is the natural frequency and ζ is the dumping factor. The two poles of transfer (14) are

$$\begin{aligned} P_{P0} &= -\zeta\omega_n + j\omega_n\sqrt{1-\zeta^2}. \\ P_{P1} &= -\zeta\omega_n - j\omega_n\sqrt{1-\zeta^2} \end{aligned} \tag{15}$$

The poles of discrete PLL form in z-plane are calculated by applying the impulse invariance method (7) mentioned above

$$\begin{aligned} Z_{P0} &= e^{P_{P0}T_{Sa}} = e^{T_{Sa}\left(-\zeta\omega_n + j\omega_n\sqrt{1-\zeta^2}\right)}. \\ Z_{P1} &= e^{P_{P1}T_{Sa}} = e^{T_{Sa}\left(-\zeta\omega_n - j\omega_n\sqrt{1-\zeta^2}\right)} \end{aligned} \tag{16}$$

T_{Sa} represents sampling period of discrete PLL system. The same procedure as in case of 1st DPLL was used and resulting formula of closed loop transfer for 2nd order DPLL was computed

$$H_{cD2ord}(z) = \begin{cases} \dfrac{z\cdot 2\left[1 - e^{-2\pi\zeta\Omega_n}\cdot\cos\left(2\pi\Omega_n\sqrt{1-\zeta^2}\right)\right] + e^{-4\pi\zeta\Omega_n} - 1}{z^2 - z\cdot 2e^{-2\pi\zeta\Omega_n}\cdot\cos\left(2\pi\Omega_n\sqrt{1-\zeta^2}\right) + e^{-4\pi\zeta\Omega_n}} & for \quad \zeta \le 1 \\ \dfrac{z\cdot 2\left[1 - e^{-2\pi\zeta\Omega_n}\cdot\cosh\left(2\pi\Omega_n\sqrt{\zeta^2-1}\right)\right] + e^{-4\pi\zeta\Omega_n} - 1}{z^2 - z\cdot 2e^{-2\pi\zeta\Omega_n}\cdot\cosh\left(2\pi\Omega_n\sqrt{\zeta^2-1}\right) + e^{-4\pi\zeta\Omega_n}} & for \quad \zeta > 1 \end{cases}. \tag{17}$$

The parameter Ω_n is defined as the normalized natural frequency relating to sampling frequency. The dumping factor has the same meaning and rate as in case of APLL. The coefficients of loop filter (see figure 3) are derived from transfer function (17)

$$k_0 = \begin{cases} \dfrac{2}{k_D k_N}\left[1 - e^{-2\pi\zeta\Omega_n}\cos\left(2\pi\Omega_n\sqrt{1-\zeta^2}\right)\right] & \zeta \le 1 \\ \dfrac{2}{k_D k_N}\left[1 - e^{-2\pi\zeta\Omega_n}\cosh\left(2\pi\Omega_n\sqrt{\zeta^2-1}\right)\right] & \zeta > 1 \end{cases} \quad for \tag{18}$$

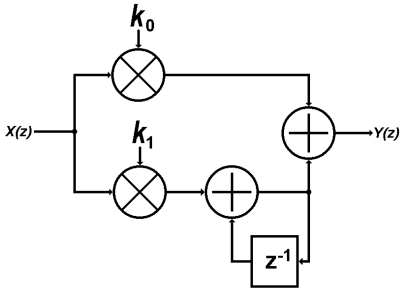

Fig. 3 Block diagram of loop filter for 2nd order DPLL

$$k_1 = \begin{cases} \dfrac{1}{k_D k_N}\left[e^{-4\pi\zeta\Omega_n} - 2e^{-2\pi\zeta\Omega_n}\cdot\cos\left(2\pi\Omega_n\sqrt{1-\zeta^2}\right) + 1\right] & \zeta \le 1 \\ \dfrac{1}{k_D k_N}\left[e^{-4\pi\zeta\Omega_n} - 2e^{-2\pi\zeta\Omega_n}\cdot\cosh\left(2\pi\Omega_n\sqrt{\zeta^2-1}\right) + 1\right] & \zeta > 1 \end{cases} \quad for \tag{19}$$

An example of frequency responses of 2nd order DPLL is shown in figure 4. There is again evident the impact of aliasing that occurs in the sampling process.

In the end, the stability of proposed discrete-time system was investigated. If the one pole in equation (15) is complex number, the second one is complex conjugate. Then one of them can be investigated and stability of 2nd order DPLL system is given by

$$\left| e^{\left(-2\pi\zeta\Omega_n - j2\pi\Omega_n\sqrt{1-\zeta^2}\right)} \right| \le 1. \tag{20}$$

This condition can be rewritten on based of exponential function properties as investigation of a real part of exponent

$$\mathrm{Re}\left\{-2\pi\zeta\Omega_n - j2\pi\Omega_n\sqrt{1-\zeta^2}\right\} \le 0 . \quad (21)$$

Analytic solution of the real part of exponent can be divided in two intervals

$$\mathrm{Re}\left\{-2\pi\zeta\Omega_n - j2\pi\Omega_n\sqrt{1-\zeta^2}\right\} = \begin{cases} -2\pi\zeta\Omega_n & \zeta \le 1 \\ \text{for} & \\ -2\pi\zeta\Omega_n - 2\pi\Omega_n\sqrt{\zeta^2-1} & \zeta > 1 \end{cases} . \quad (22)$$

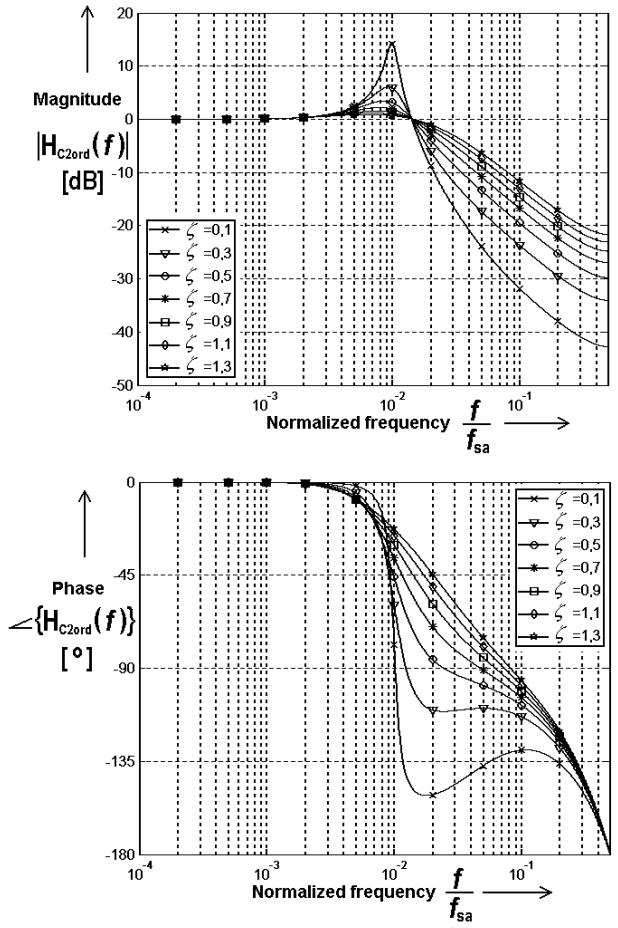

Fig. 4 Close loop frequency responses of 2nd order DPLL ($\Omega_n = 0.01$)

Because of the normalized natural frequency Ω_n and the dumping factor ζ are always positive the condition (21) is fulfilled at all times and this configuration of 2nd order DPLL is also unconditionally stable.

V. Conclusion

In the paper an analyses of discrete form of phase locked loops was executed. Crucial aspect of resulting analyses is that the aliasing originating in sampling process affects the characteristics of DPLL or DDLL, especially in fast loops. It is important for a design of narrow band systems, where the fluctuation of tracked quantities could be sizable, as in satellite or deep-space communication.

Because the close loop transfer is corresponding to transfer of low-pass filter with unity gain in pass-band, the error function has to have a character of high-pass filter with the same cut-off frequency as the close loop. The result of this is that the phase drift with low-frequency components do not take effect on phase error. On the contrary, the fast phase drift has more significant impact on phase error.

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