

Low Complexity Regular LDPC codes for Magnetic Storage Devices

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Abstract—LDPC codes could be used in magnetic storage devices because of their better decoding performance compared to other error correction codes. However, their hardware implementation results in large and complex decoders. This one of the main obstacles the decoders to be incorporated in magnetic storage devices. We construct small high girth and rate 2 column-weight codes from cage graphs. Though these codes have low performance compared to higher column weight codes, they are easier to implement. The ease of implementation makes them more suitable for applications such as magnetic recording. Cages are the smallest known regular distance graphs, which give us the smallest known column-weight 2 codes given the size, girth and rate of the code.

Keywords— Structured LDPC codes, cage graphs.

I. INTRODUCTION

LOW-density parity-check (LDPC) codes have been shown to perform close to the Shannon limit. It was proved in [1] that LDPC codes with column weight (number of 1's in code matrix column) $j \geq 3$ have a minimum distance that grows linearly with the block length (number of columns) n for given j and row-weight (number of 1's in matrix row) k and that the minimum distance for codes with $j = 2$ grows logarithmically with n . However, compared with $j \geq 3$ codes, codes with $j = 2$ are easier to implement and require less storage making them a target for applications such as magnetic recordings [2]. It is also reported that codes with column weight of 2 exhibits block error statistics more compatible with an outer Reed-Solomon (RS) code.

Reed-Solomon(R-S) codes are widely used in current storage devices, mainly because of their relatively low hardware-complexity and high capacity to detect and correct burst errors. They also lend themselves to high-speed encoding and decoding required for high bandwidth disk drives [3]. These applications require short codeword lengths, which allow easier encoding, less implementation memory and low decoding complexity. LDPC codes offer significant performance advantage over R-S codes; however, it comes at

the expense of increased complexity. LDPC codes can be used as second level codes in concatenated error correction architectures as shown in Figure 1 [2]. For this architecture to be practical we need small decoder VLSI to fit both encoder and decoder making it easier to integrate in magnetic storage devices. LDPC codes with column weight of 2 have low implementation complexity and good performance for magnetic recording applications[2].

There are several ways of constructing column-weight 2 LDPC codes. In [2], 4 and 6 cycle-free codes are constructed

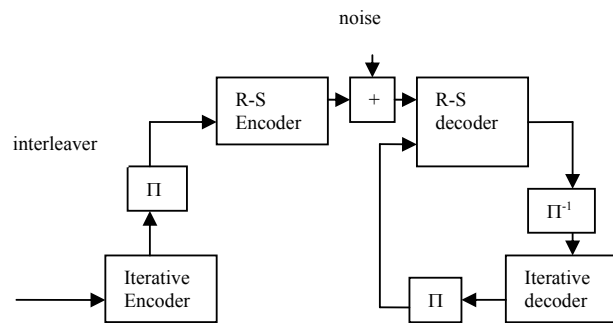


Fig. 1 Serial concatenation of partial response channel encoding and decoding

using disjoint difference sets and in [4] codes with large girth are constructed based on geometry. Though the codes in [4] have large girth, they are not the smallest. The construction method also does not produce high girths and rates codes. For example, codes of girths 16 and 20 are of rate 1/3. In this paper we construct low complexity codes that could be incorporated in magnetic storage devices from cage graphs, with high girth and high rates. Since cages are the smallest known graphs of a given vertex degree and girth, the resulting codes are the smallest one could get for the same girth and vertex degree.

This paper is organized as follows. Section II describes cages and construction of codes based on cages. Section III concludes.

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B. Hardware Implementation

Structured codes reduce hardware complexity both in the encoder and decoder. The structure or pattern in the code makes it easier to multiply elements of the generator matrix. The cage graph of figure 3 produces a 12x36 code matrix with a girth of 8. The matrix has a defined structure in that odd vertices are connected to even vertices and vice versa. As an example the edges (columns) could be divided into six groups as shown in figure 4. Edges from each odd vertex could form a group. By doing that we get 6 groups of 6 edges each. A similar division with edges from even vertices works in a similar way. In figure 4 columns (edges) for each row (vertex) are treated as a group. In each group connections are between the odd row and all even rows. So the connections could be calculated rather than storing the destination addresses. The grouping reduces the number of interconnections. The number of groups is much smaller than the number of individual rows or columns. Structuring also simplifies addressing. Addresses are generated according to the code pattern. The addressing in each group is determined by the pattern, which are all odd or even rows. In random codes the random communication makes exchange of messages between processing nodes complicated. If the communication network is not hardwired an address table is needed.

Column-weight 2 codes simplify the encoder and decoder complexity further by reducing the number of elements in the code matrix. This means less computations and memory in the encoder. Besides reduced memory, the variable nodes (column computations) complexity of the decoder is reduced. The variable node computation involves the summation of the incoming messages and the channel estimate of the information (received) bit. With two incoming messages, the computation is reduced to exchanging incoming messages and adding them to the channel estimation before sending them as outgoing messages.

However, as noted above, cage graphs are not constructed with one method. Therefore their structure will differ from graph to graph. It is important then to analyze each graph to best exploit its structure for hardware implementation. Decoding performance characteristics for each graph also need to be analyzed before implementation.

III. CONCLUSION

An approach for constructing LDPC codes with column weight of 2 has been described. Cage graphs are used to represent the code matrix, where vertices are rows and edges are columns. Since cages are the smallest known regular graphs of a given girth and valency, the resulting codes are the smallest one could obtain. These codes have low implementation costs and could therefore be incorporated in magnetic storage devices. Non-regular distance graphs could also be used to construct column-weight 2 codes in a similar way. The resulting codes would have varying rows valencies.

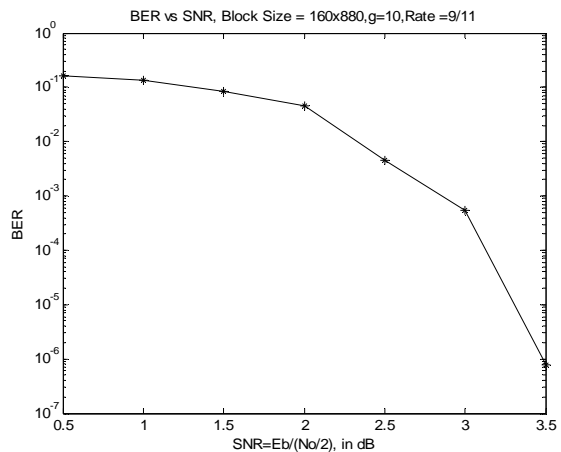


Fig. 5 BER performance curve of a (2,11) code with g=10

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