International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:6, No:1, 2012

A Design of Electronically Tunable Voltage-mode Universal Filter with High Input Impedance

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***Abstract*—**This article presents a voltage-mode universal biquadratic filter performing simultaneous 3 standard functions: low-pass, high-pass and band-pass functions, employing differential different current conveyor (DDCC) and current controlled current conveyor (CCCII) as active element. The features of the circuit are that: the quality factor and pole frequency can be tuned independently via the input bias currents: the circuit description is very simple, consisting of 1 DDCC, 2 CCCIIs, 2 electronic resistors and 2 grounded capacitors. Without requiring component matching conditions, the proposed circuit is very appropriate to further develop into an integrated circuit. The PSPICE simulation results are depicted. The given results agree well with the theoretical anticipation.

***Keywords*—**Filter, DDCC, CCCII, Analog circuit, Voltage-mode, PSPICE

I. INTRODUCTION

AN analog filter is an important building block, widely used for continuous-time signal processing. It can be found in many fields: including, communications, measurement, and instrumentation, and control systems [1-2]. Moreover, it is also used in ultracapacitor-battery hybrids for vehicular applications [3]. One of most popular analog filters is a universal biquadratic filter, since it can provide several functions in the same topology.

The literature surveys show that the voltage-mode universal filter circuits [4-13], have been reported. Unfortunately, these reported circuits suffer from one or more of following weaknesses:

- Excessive use of the passive elements, especially external resistors [4, 5, 6, 8, 11, 12].
- Require changing circuit topologies to achieve several functions [7, 9, 11].
- Lack of electronic adjustability [4, 5, 6, 7, 8, 9, 10, 11, 12].
- Cannot provide simultaneous low-pass, high-pass, and band-pass functions [4-6, 8, 10].
- The pole frequency and quality factor cannot be tuned independently [9-10, 13].

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The aim of this paper is to propose a voltage-mode universal biquadratic filter, emphasizing on use of DDCC and CCCIIs with grounded elements. The features of proposed circuit are that: the proposed universal filter can provide simultaneous 3 standard functions (low-pass, high-pass and band-pass) without changing circuit topology: the circuit description is very simple, it uses 1 DDCC, 1 CCCIIs, 2 electronic resistors and 2 grounded capacitors, which is suitable for fabricating in mono2lithic chip: quality factor and pole frequency can be independently/electronically adjusted. The performances of proposed circuit are illustrated by PSPICE simulations; they show good agreement as mentioned.

II. THEORY AND PRINCIPLE

A. Basic concept of DDCC

The electrical behaviors of the ideal DDCC are represented by the following hybrid matrix [14]:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_Z \end{bmatrix}. \tag{1}$$

The symbol and the equivalent circuit of the DDCC are illustrated in Figs. 1(a) and (b), respectively.

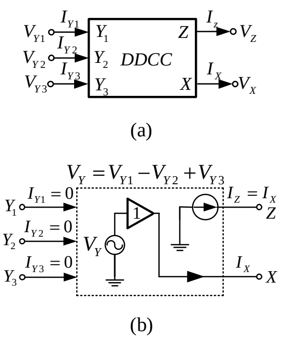

Fig. 1 DDCC (a) Symbol (b) Equivalent circuit

B. Basic Concept of CCCII

Typically, the CCCII is a versatile analog building block which is similar to the conventional current conveyor (CCII) except that the CCCII has a finite input resistance R_X at the X terminal. CCCII has the advantage of electronically adjustability over the CCII, because it allows the adjustment of R_X via the bias current I_B. The relationship between the voltage and current variables among X, Y and Z ports of an ideal CCCII can be described by

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}, \qquad (2)$$

where R_x is the parasitic resistance at x terminal. For a CMOS CCCII, the R_x can be expressed as

$$R_x = \sqrt{\frac{1}{kI_B}};\ k = 8\mu_n C_{ox}\left(\frac{W}{L}\right)_{10-11} = 8\mu_n C_{ox}\left(\frac{W}{L}\right)_{12-13}. \qquad (3)$$

Here k is the physical transconductance parameter of the MOS transistor. The symbol and the equivalent circuit of the CCCII are illustrated in Figs. 2(a) and (b), respectively.

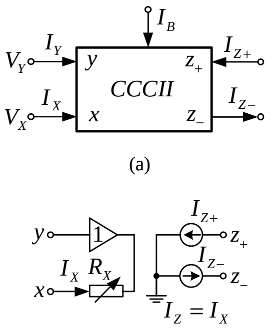

Fig. 2 CCCII (a) Symbol (b) Equivalent circuit

C. Proposed Voltage-Mode Universal Filter

The proposed filter is shown in Fig. 3. It is seen that proposed circuit consists of 1 DDCC, 2 CCCIIs, 2 electronic resistors and 2 grounded capacitors which is easy to fabricate. Moreover, the proposed circuit can provide high input impedance that can be cascaded in voltage-mode circuit. The transresistance of the electronic resistor circuit can be expressed as [15]

$$R_K = \frac{V_{in}}{I_{in}} = \frac{L}{2\mu C_{OX} W\left(V_{DD} - V_T\right)}. \qquad (4)$$

where V_T denotes the threshold voltage. It is found that the proposed circuit can respectively provide bandpass, higpass and lowpass responds with following transfer functions:

$$T(s)_{BP} = \frac{V_{BP}}{V_{in}} = \frac{s\dfrac{R_2}{C_1R_1R_{x2}}}{s^2 + s\dfrac{R_2}{C_1R_1R_{x2}} + \dfrac{1}{C_1C_2R_1R_{x1}}} \qquad (5)$$

$$T(s)_{HP} = \frac{V_{HP}}{V_{in}} = \frac{s^2}{s^2 + s\dfrac{R_2}{C_1R_1R_{x2}} + \dfrac{1}{C_1C_2R_1R_{x1}}}, \qquad (6)$$

$$T(s)_{LP} = \frac{V_{LP}}{V_{in}} = \frac{\dfrac{1}{C_1C_2R_1R_{x1}}}{s^2 + s\dfrac{R_2}{C_1R_1R_{x2}} + \dfrac{1}{C_1C_2R_1R_{x1}}}. \qquad (7)$$

From Eqs. (5)- (7), the pole frequency (ω_0) and quality factor (Q_0) can be written as

$$\omega_0 = \sqrt{\frac{1}{C_1C_2R_1R_{x1}}}, \qquad (8)$$

$$Q_0 = \frac{R_{x2}}{R_2}\sqrt{\frac{C_1R_1}{C_2R_{x1}}}. \qquad (9)$$

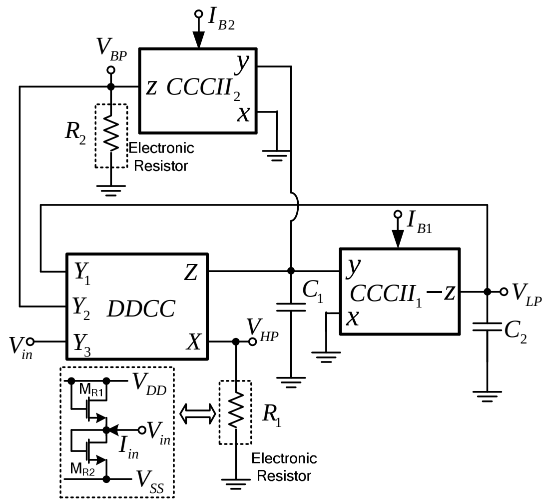

Fig. 3 Proposed voltage-mode universal filter

If $R_{xi} = 1/\sqrt{kI_{Bi}}$, the pole frequency and quality factor can be rewritten as

$$\omega_0 = \sqrt{\frac{\left(kI_{B1}\right)^{\frac{1}{2}}}{C_1C_2R_1}}, \qquad (10)$$

$$Q_0 = \frac{1}{R_2\sqrt{kI_{B2}}}\sqrt{\frac{C_1R_1\left(kI_{B1}\right)^{\frac{1}{2}}}{C_2}}. \qquad (11)$$

It is found from Eqs. (10) and (11) that the quality factor can be adjusted independently from the pole frequency by varying I_{B2}.

III. Simulation Results

To investigate the theoretical analysis, the proposed filter in Fig. 3 is simulated by using the PSPICE simulation program. Internal constructions of DDCC and CCCII used in simulation are respectively shown in Figs. 4 and 5, respectively. The PMOS and NMOS transistors have been simulated by respectively using the parameters of a 0.25μm TSMC CMOS technology [15]. The transistor aspect ratios of PMOS and NMOS transistor are indicated in Table I. The circuit was biased with ±1.5V supply voltages, VBB=-0.6V, $C_1=C_2$=0.1nF, I_{B1}=50μA and I_{B2}=25μA. It yields the simulated pole frequency of 1.35MHz. The result shown in Fig. 6 is the gain responses of the proposed biquad filter obtained from Fig. 3. This clearly shows that the proposed biquad circuit can provide simultaneous low-pass, high-pass and band-pass functions without modifying circuit topology. Fig. 7 display gain responses of band-pass function, with different I_{B2} values. It is indicated that the quality factor can be tuned by I_{B2} without affecting the pole frequency as shown in Eq. 11. The transient response of the proposed filter from band-pass function for center frequency of 1.35MHz can be seen in Fig. 8.

TABLE I
Dimensions Of The Transistors

Transistors	W(μm)	L(μm)
M1-M4, M19-M20	3	0.25
M5-M8	1	0.25
M9-M10	10	0.25
M13-M16, M18-M19	5	0.5
M17	5.5	0.5
M20-M21	16	0.25
M22-M23	8	0.25
M24-M26, M28-M29	15	0.5
M27	14.5	0.5
MR1-MR2	2.2	1

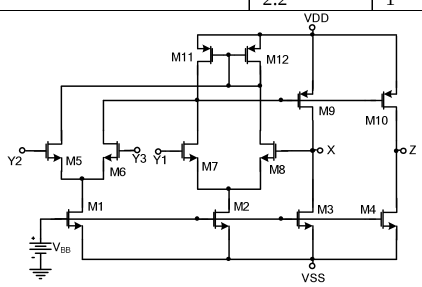

Fig. 4 Internal construction of DDCC

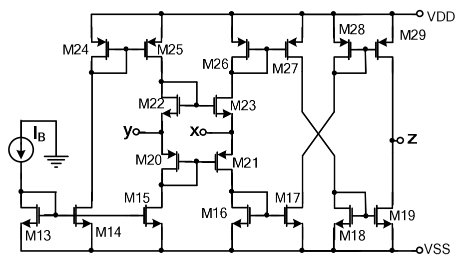

Fig. 5 Internal construction of CCCII

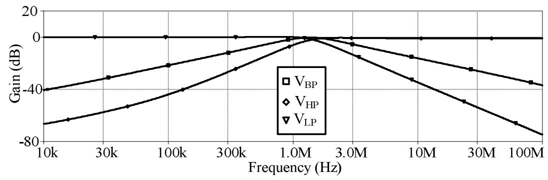

Fig. 6 Gain responses of universal filter

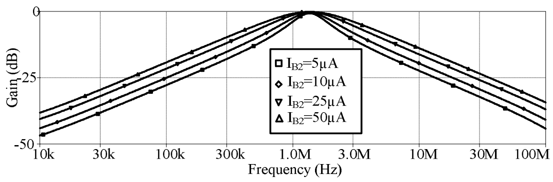

Fig. 7 Band-pass responses for different values of I_{B2}

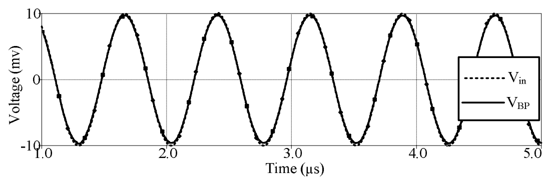

Fig. 8 Transient response of band-pass function

IV. Conclusion

The voltage-mode universal biquadratic filter based on DDCC and CCCII has been presented. The advantages of the proposed circuit are that: it performs low-pass, high-pass, and band-pass functions from the same circuit configuration without component matching conditions: the quality factor and the pole frequency can be independently controlled via input bias current, which is easily modified to use in control systems or vehicular systems by using a microcontroller. The circuit description comprises 1 DDCC, 2 CCCIIs, 2 electronic resistors and 2 grounded capacitors, which is attractive for IC implementation.

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ISSN: 2517-9438
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