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A Low Voltage High Performance Self Cascode Current Mirror

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***Abstract*—**A current mirror (CM) based on self cascode MOSFETs low voltage analog and mixed mode structures has been proposed. The proposed CM has high output impedance and can operate at ± 0.5 V. P-Spice simulations confirm the high performance of this CM with a bandwidth of 6.0 GHz at input current of 100 μA.

***Keywords*—**Current Mirrors, Composite Cascode Structure, Current Source/Sink.

I. Introduction

MANY low voltage design techniques have been developed to meet the needs of present era of low power portable electronic equipment, which drove the analog designers to look for innovative design techniques like self cascode MOSFETs [1-5]. In this paper, we have investigated the merits and demerits of self cascode approach. For this aim in mind we designed a CM based on self cascode MOSFETs and analyzed its various properties through the p-spice simulations for 0.13 micron CMOS technology.

II. Cascode Structures

The idea behind cascode structure is to convert the input voltage to a current and apply the result to a common source stage. This has been employed in various LV topologies [6-10]. In 2004, Comer [11-12] discussed the effects on the overall composite cascode circuit performance with one device operating in the sub threshold and the other device operating in the active region and suggested that this approach may result in a very high gain stage for use in op-amps, along with low power dissipation too [13,14].

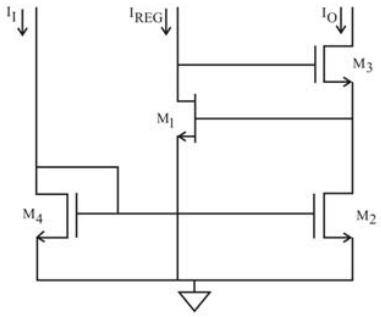

Fig. 1 Regulated cascode CM

The idea of cascode structure is employed in regulated cascode [15,16] to increase the output resistance to $g_m^2 r_{ds}^3$ (Fig. 1) and the implementation requires CMOS technology as the regulated cascode structure requires both PMOS and NMOS transistors. Fig. 2 is called "folded cascode", used to alleviate the drawback of telescopic cascode's, limited output swings and difficulty in shorting the input and output [16,17].

Primary advantage of folded structure lies in the choice of the voltage levels because it does not "stack" the cascade transistor on top of the input device. However, this structure generally consumes higher power.

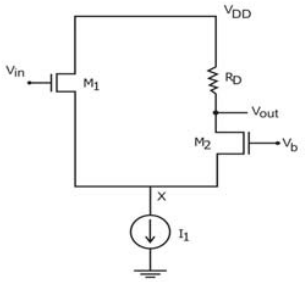

Fig. 2 Folded cascade

The Composite Cascode Connection: It is seen that there are two distinct advantages of using cascode structures. Firstly, it provides higher output impedance and secondly, it reduces the effect of miller capacitance on the input of the amplifier. A Low Voltage Current Mirror (LVCM) based on level shifter approach was proposed that required a low bias voltage of order of ± 1.0V [18,19]. This paper proposes a LV high performance CM structure that applies composite cascode connections, proposed by Comer.

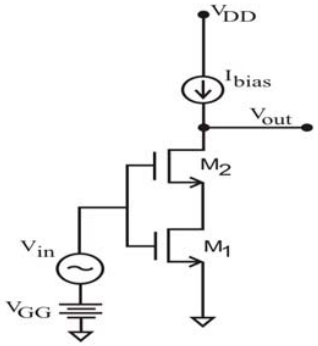

Fig. 3 Composite Cascode

The structure shown in Fig. 3, has both the gates of M1 & M2 driven by the input signal and share a single bias source V_{GG}. If M2 and M1 have similar *W/L* ratio, then M1 will operate in the triode region while M2 will operate in the active region. In this case, the composite cascode works like a common-source stage, but with higher voltage gain. If M2 is chosen with higher aspect ratio then M1, with appropriate bias of V_{GG} and I_{bias}, M1 is placed in the strong inversion region while M_2 is operating in the weak inversion region. The gain in this case is further increased.

Assuming the current source has infinite output impedance, the output resistance is $r_{out} = r_{ds1} + r_{ds2} + (g_{m2} + g_{mb2})\, r_{ds1}\, r_{ds2}$ [20]. The benefit of this conventional cascode technique is its high output impedance. Its drawbacks are limited input common mode range, small output swing and relatively high power supply requirements [21, 22].

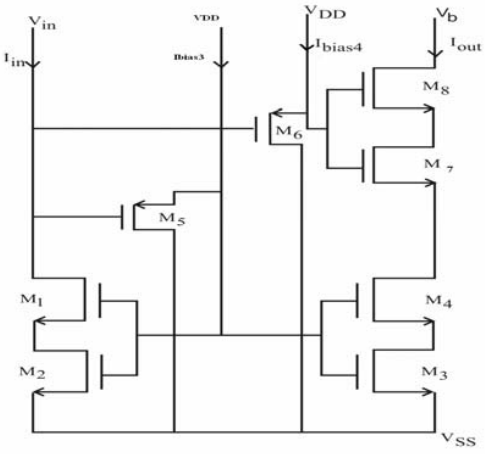

Fig. 4 Self Cascode LVCM

If this conventional cascode structure is changed to bias the upper MOS device M_2 in a way that there is less effect on the output voltage swing, the output impedance of the connection may be increased with sufficient output swing at low supply voltage. One practice is to make both the gates of M1 & M2 driven by the input signal and share a single bias source. This approach results in high output impedance originating due to the degeneration of the source of M2. This composite cascode approach, which combines the regular active devices with weak inversion devices, is a promising low voltage design technique discussed in detail in this paper.

Proposed Self cascode CM (SCLVCM):

The proposed LVCM is shown in Fig. 4. M1 & M2, M3 & M4, M7 & M8 are pairs of composite cascode structures. They have replaced M1, M2 & M3 of LVCM [19]. The aspect ratios of different transistors are given in Table I. The circuit is simulated for 0.13 µm technology with level 3 parameters. Ibias3 and Ibias4 are assumed to be 1nA and 100µA respectively. The selection criterion for Ibias3 is to ensure lower $V_{in.}$ Ibias4 is selected to ensure ON condition for M6. All the circuit operations are simulated for supply voltage of ± 0.5 V.

Simulation Results: The current transfer characteristics are shown in Fig. 5 and its input characteristics in Fig. 6. The effect of gate résistance over bandwidth is shown in Fig.7. The gate resistance RG is connected between the cascode pairs M1 & M2 and M3 & M4. For I_{in} of 100 µA the 3db bandwidth comes out to be 6.02 GHz. The bandwidth for I_{in} of 250µA is 6.4 GHz and for I_{in} of 300 µA is 10.2 GHz. Thus bandwidth is shown to be a function of I_{in}.

The influence of various compensation techniques over the bandwidth are shown in Fig. 8. The gate resistance of 1.5KΩ (RG) degrades the bandwidth from 6.02 GHz to 5.75 GHz and that of 3KΩ degrades it to 5.5 GHz. The capacitor (C) also degrades the bandwidth to 2.39 GHz. There is an improvement in bandwidth only when both Resistance and Capacitor are included, it comes out to be 4.7 GHz. Hence, for this structure the compensation techniques (RG and C) are not required.

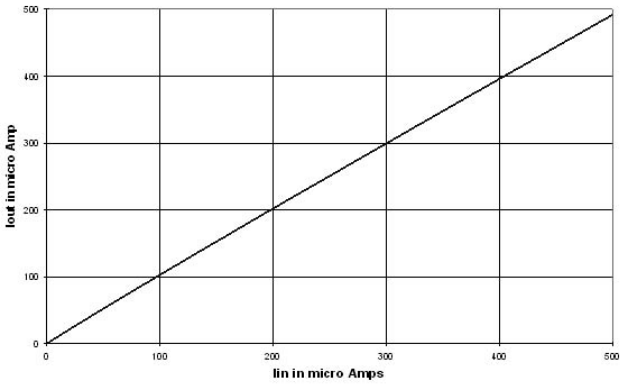

Fig. 5 Current Transfer Characteristics

The small signal transfer analysis of this circuit at 100 µA gave the current gain, i.e. $I_{out}/ I_{in} = 1$, input resistance as 1KΩ and output resistance as 9 MΩ, with the power dissipation of 0.3 mW. However, for I_{in} of 300 µA, the current gain changes to 0.9, input resistance to 900 Ω and output resistance to 2 MΩ.

The power dissipation for this is 0.7 mW. The output current to applied drain bias characteristics of M8 (V_b) is shown in Fig. 9 for the proposed self cascode LVCM of Fig. 4. Fig. 10 shows the characteristics for high currents. The dependency of output current swing on V_b is seen at low currents.

TABLE I
W/L FOR VARIOUS TRANSISTORS

MOSFETS	TYPE	W/L(µm/µm)
M1,M4,M8	NMOS	26/0.13
M2,M3,M7	NMOS	1.95/0.13
M5,M6	PMOS	1.95/0.13

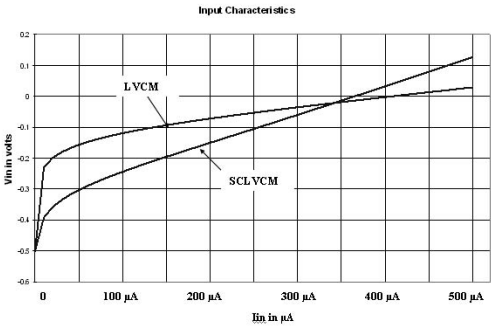

Fig. 6 Input Characteristics of SCLVCM

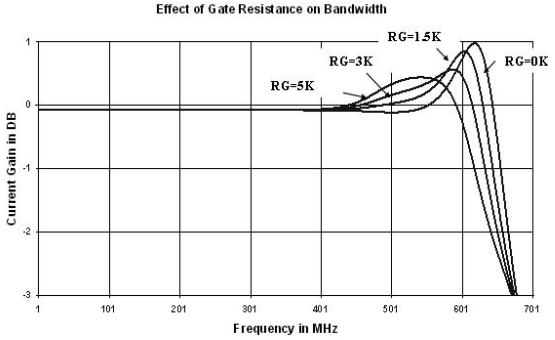

Fig. 7 Effect of gate resistance over the bandwidth of SCLVCM

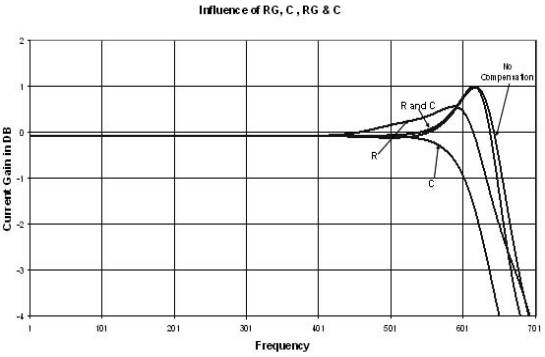

Fig. 8 Influence of RG and C, over the bandwidth of SCLVCM

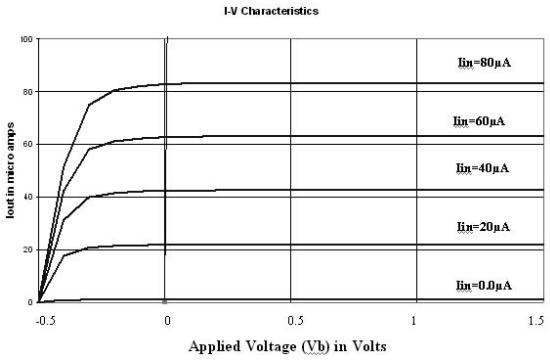

Fig. 9 *I-V* Characteristics of proposed SCLVCM at low currents

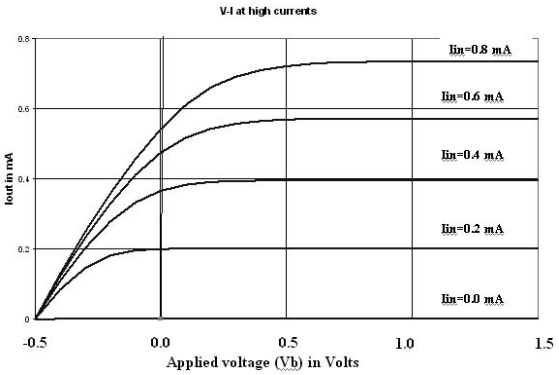

Fig. 10 I-*V* Characteristics of proposed SCLVCM at high currents

III. Conclusion

The self cascode LVCM presented here can be used as a high performance Current Sink and Source having an output resistance of 9 MΩ. This approach of increasing the (*W/l*) aspect ratios works effectively at low bias voltage V_{in} of ± 0.5 V. Its high bandwidth (6.02 GHz) without any additional components makes it quite attractive for biasing analog circuits requiring high output resistance and gain. Hence can be used as load resistances in CM circuits. They can extensively be used where power supply requirements are not the constraint and that high output resistance is of utmost importance.

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